(USAF) T.O. 33D7-24-13-2

(FAA) FAA TI6360.45

(NAVY) NAVELEX 0967-429-6010

PRELIMINARY
TECHNICAL MANUAL

SERVICE

TEST SET, VIDEO SIGNAL PROCESSOR AN/TPM-32

PART NO. 374571-1

(AIL, a division of Cutler-Hammer)

F33657-70-C-0207

PUBLISHED UNDER AUTHORITY OF THE SECRETARY OF THE AIR FORCE

15 NOVEMBER 1971

Reproduction for nonmilitary use of the information or illustrations contained in this publication is not permitted without specific approval of the issuing service. The policy for use of Classified Publications is established for the Air Force in AFR 205-1.

Technical orders are normally distributed promptly after printing. Date(s) shown on the title page (lower right corner) are for identification only. This is not a distribution date. Processing time sometimes causes distribution to only appear to have been delayed.

LIST OF EFFECTIVE PAGES

INSERT LATEST CHANGED PAGES. DESTROY SUPERSEDED PAGES.

NOTE: The portion of the text affected by the changes is indicated by a vertical line in the outer margins of the page. Changes to illustrations are indicated by miniature pointing hands. Changes to wiring diagrams are indicated by shaded areas.

Dates of issue for original and changed pages are:
Original . 0 .

TOTAL NUMBER OF PAGES IN THIS PUBLICATION IS 111 CONSISTING OF THE FOLLOWING:

Page No.	*Change No.*
Title	0
A	0
i thru vii	0
1-0 thru 1-7	0
2-1 thru 2-9	0
3-1 thru 3-12	0
4-1 thru 4-47	0
5-1 thru 5-26	0

Upon receipt of the second and subsequent changes to this technical order, personnel responsible for maintaining this publication in current status will ascertain that all previous changes have been received and incorporated. Action should be taken promptly if the publication is incomplete.

* The asterisk indicates pages changed, added or deleted by the current change.

ADDITIONAL COPIES OF THIS PUBLICATION MAY BE OBTAINED BY USAF ACTIVITIES IN ACCORDANCE WITH T.O. 00-5-2

USAF

T.O. 33D7-24-13-4

PRELIMINARY
TECHNICAL MANUAL

ILLUSTRATED PARTS BREAKDOWN

TEST SET, VIDEO SIGNAL PROCESSOR AN/TPM-32

PART NO. 374571-1

(AIL, a division of Cutler-Hammer)

F33657 70-C-0207

PUBLISHED UNDER AUTHORITY OF THE SECRETARY OF THE AIR FORCE

1 NOVEMBER 1971

CHANGE 1 29 JANUARY 1972

TABLE OF CONTENTS

Section		Page
	CHAPTER 1. GENERAL INFORMATION	
	1-1. Description and Purpose	1-1
	1-5. Leading Particulars	1-1
	1-7. Capabilities and Limitations	1-1
	1-9. Equipment Supplied	1-2
	1-11. Equipment Required But Not Supplied	1-7
	CHAPTER 2. INSTALLATION	
I	INSTALLATION PLANNING	2-1
	2-1. Location	2-1
	2-4. Environmental Consideration	2-2
	2-6. Power Requirements	2-2
	2-8 Special Tools Required	2-2
II	LOGISTICS	2-3
	2-10. Receiving Data	2-3
	2-12. Unpacking	2-3
	2-14. Inspection	2-3
	2-16. Transportability	2-3

TABLE OF CONTENTS (Cont)

Section

III INSTALLATION PROCEDURES 2-5

2-18. General 2-5

2-20. General Installation Instructions 2-5

IV PREPARATION FOR RESHIPMENT 2-9

CHAPTER 3. OPERATION

I CONTROLS AND INDICATORS 3-1

II OPERATION PROCEDURES 3-10

3-3. Starting Procedures 3-10

3-5. Operating Procedures 3-10

III EMERGENCY OPERATION (Not Applicable) 3-12

CHAPTER 4. PRINCIPLES OF OPERATION

I FUNCTIONAL SYSTEM OPERATION 4-3

4-2. Overall Functional Block Diagram Discussion 4-3

II FUNCTIONAL OPERATION OF ELECTRONIC CIRCUITS . . 4-7

4-11. TRU Output Functional Group 4-7

4-67. Azimuth Register Group 4-40

4-69. Transfer Register Group 4-41

4-72. Target and Reply Register Transfer Group 4-42

TABLE OF CONTENTS (Cont)

Section		Page
	4-78. Power Distribution Circuits	4-45
	4-80. Manual Clearing and Monitoring Circuits	4-47
	CHAPTER 5. MAINTENANCE	
I	ORGANIZATION/FIELD MAINTENANCE	5-1
	5-2. Scope	5-1
	5-5. Maintenance Test Equipment	5-2
	5-7. Test Points	5-2
	5-9. Performance Test and Fault Isolation Procedures	5-5
	5-11. Complete Performance Test	5-6
	5-13. How To Use The Diagnostic Flow Chart	5-6
	5-19. DC Voltage Requirements and Sources	5-24
	5-21. Alignment and Adjustment Procedures	5-25
II	SPECIAL MAINTENANCE (Not Applicable)	5-26

LIST OF ILLUSTRATIONS

Number	Title	Page
1-0	Test Set, Video Signal Processor AN/TPM-32	1-0
3-1	Test Set, Video Signal Processor AN/TPM-32, Front Panel Controls, Indicators and Connectors	3-2
3-2	Test Set, Video Signal Processor AN/TPM-32, Rear Panel Controls and Connectors	3-8
3-3	Video Signal Processor, CP-1045/T, Performance Test Setup Diagram	3-11
4-1	Test Set, Video Signal Processor AN/TPM-32, Overall Block Diagram	4-2
4-2	Target Reporting Unit Output Circuits, Block Diagram	4-8
4-3	FSK Receiver Input/Output and Clock Timing Diagram	4-11
4-4	Input Test Message, FSK Coded Format	4-12
4-5	Timing Sequence of Target and Reply Transfer Strobe Inputs	4-15
5-1	Performance Tests and Fault Isolation Procedures, Flow Diagram	5-7

LIST OF TABLES

Number	Title	Page
1-1	Leading Particulars	1-2
1-2	Capabilities and Limitations	1-3
1-3	Equipment Supplied	1-5
2-1	Shipping Container Contents	2-4
2-2	Cabling Requirements	2-7
3-1	Video Signal Processor AN/TPM-32 Test Set Front Panel Controls, Indicators and Connectors	3-3
3-2	Video Signal Processor, AN/TPM-32, Test Set Rear Panel Controls and Connectors	3-9
5-1	Maintenance Test Equipment	5 -2
5-2	Test Points	5 -3

INTRODUCTION

This manual contains service instructions for Test Set, Video Signal Processor AN/TPM-32 used to interface with AN/TPX-42A(V) Interrogator Set Video Signal Processor CP-1045/T to provide on-line testing or test bench monitoring of the Video Signal Processor. The primary function of the test set is to display the contents of the Video Signal Processor Memory, Target Reporting Unit (TRU), Azimuth Register, Transfer Register, Target Register and Reply Register.

The Video Signal Processor Test Set has been developed and manufactured by AIL, a division of Cutler-Hammer, located in Deer Park, Long Island, New York, 11729.

This manual is arranged in five chapters. A brief description of each chapter contained herein follows:

Chapter 1, General Information, contains a brief description of the equipment and its purpose, functional characteristics, and lists of equipment supplied and equipment required but not supplied.

Chapter 2, Installation, contains installation planning, logistics, installation procedures and reshipment information.

Chapter 3, Operation, includes a description of all controls and indicators and information necessary for operating the test set.

Chapter 4, Principles of Operation, contains a functional description of operation of the Video Signal Processor Test Set and a detailed description of electronic circuits.

Chapter 5, Maintenance, provides instructions and procedures at the organizational and field level, special maintenance instructions, performance test standards and diagnostics.

Additional technical orders associated with this technical manual are the following:

T.O. 33D7-24-13-3	Circuit Diagrams
T.O. 33D7-24-13-4	Illustrated Parts Breakdown

Applicable publications governing the use of abbreviations, symbols and reference designations, used in this technical manual are as follows:

MIL-STD-12	Abbreviations
MIL-STD-15-1	Graphic Symbols for Electronic Diagrams
MIL-STD-806	Graphic Symbols for Logic Diagrams
ASA Y32.16	Electronic Reference Designations

The following technical service manuals provide extended coverage on the components of the Test Set, Video Signal Processor AN/TPM-32 when they are removed from the test set for testing.

T.O. 33D7-49-55-2	Test Set, Electronic Circuit Plug-In Unit
T.O. 33D7-6-24-2	Test Set, Power Supply

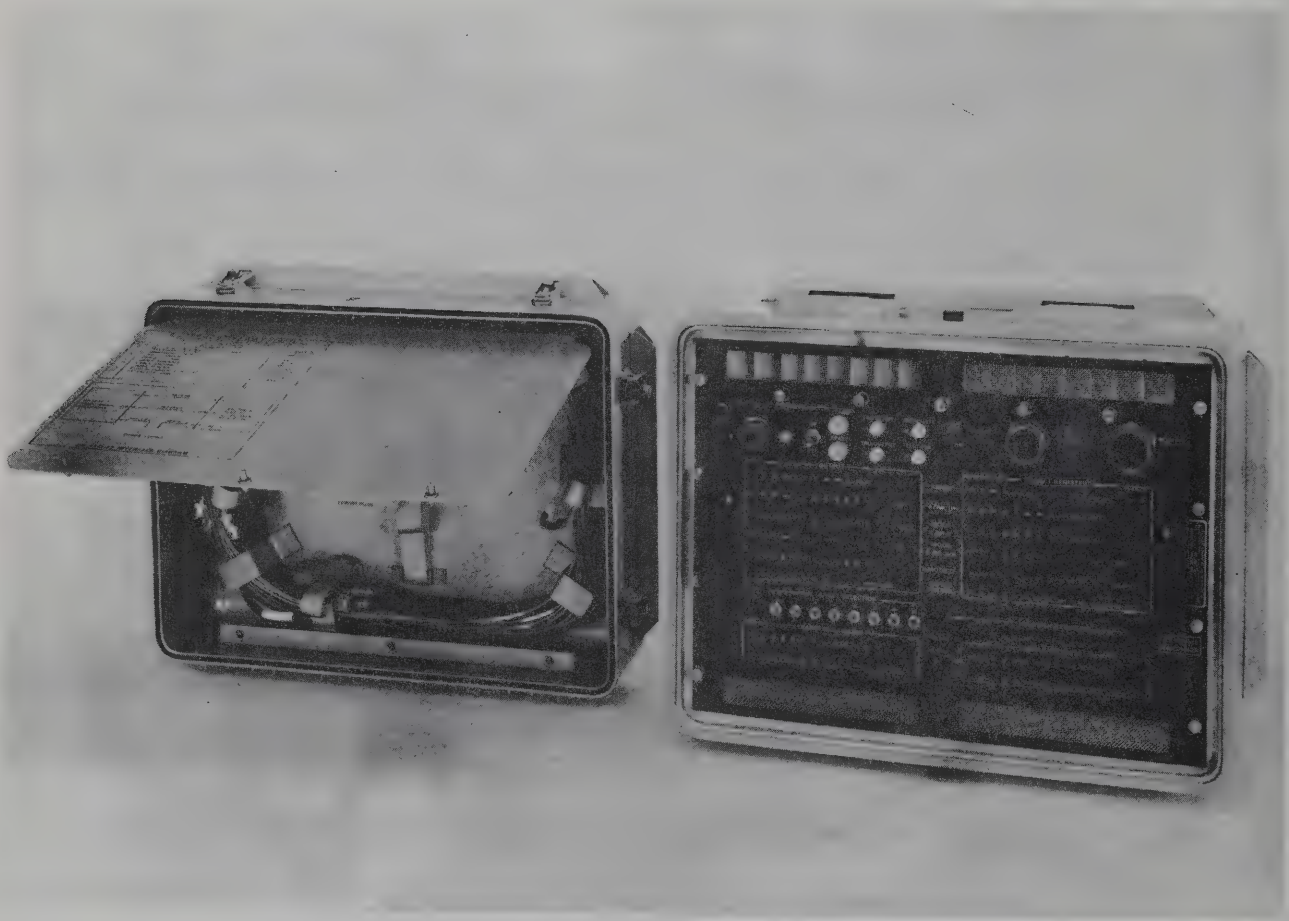


Figure 1-0. Test Set, Video Signal Processor AN/TPM-32

CHAPTER 1

GENERAL INFORMATION

1-1. DESCRIPTION AND PURPOSE.

1-2. The Test Set, Video Signal Processor AN/TPM-32 (here after referred to as test set) provides bench testing and on-line monitoring of the Video Signal Processor CP-1047/T. The test set contains a power supply and a total of 38 circuit boards. The printed circuit boards are comprised of eight basic types. The test set is mounted in a combination case which permits its use as a portable instrument. The test set is used in either a test mode or a normal on-line mode of operation.

1-3. In the test mode, the video signal processor provides a series of test messages, data bits, control and miscellaneous signals to permit the test set to monitor and display the functioning of specific circuits within the video signal processor. The specific circuits are: memory target detection unit (TDU), reply detection unit (RDU), azimuth increment, and transfer buffers circuits.

1-4. In the normal on-line mode, the test set functions the same as in the test mode except the video signal processor supplies the test set with real target information instead of test messages.

1-5. LEADING PARTICULARS.

1-6. The leading particulars of the test set are given in table 1-1.

1-7. CAPABILITIES AND LIMITATIONS.

1-8. The capabilities and limitations of the test set are given in table 1-2.

1-9. EQUIPMENT SUPPLIED.

1-10. Table 1-3 lists the equipment supplied with the test set.

Table 1-1. Leading Particulars

PRIMARY POWER REQUIREMENTS	
Input power	105-132 volts single phase 45-65 Hz or 380-420 Hz.
Power consumption	150 watts maximum
PHYSICAL CHARACTERISTICS	
Weight	100-pounds max.
Dimensions (inches)	
Height	18 max.
Width	24 max.
Depth	18 max.

Table 1-1. Leading Particulars (Cont)

TRANSPORTABILITY

There are no transportability requirements peculiar to this test set.

STORAGE

There are no storage requirements peculiar to this test set.

OVERLOAD PROTECTION

-5 Vdc supply has current limiting protection.

+5 and +12 Vdc supplies have current foldback protection which protect the circuits against 115% overload.

Table 1-2. Capabilities and Limitations

ENVIRONMENTAL CONSIDERATIONS	
Ambient temperature	
Operating	32°F to 125°F (0°C to +52°C)
Non-operating	-79.6°F to +159°F (-62°C to +71°C)
Altitude	
Operating	0 to 10,000 feet
Non-operating	0 to 50,000 feet
Humidity	
Operating and non-operating	up to 95 ±5% including condensation

Table 1-2. Capabilities and Limitations (Cont)

FUNCTIONAL CHARACTERISTICS	
Digital output message	
Amplitude	2.5 to 5.0 volts
Polarity	Positive
Frequency	25 kHz
Rise Time	1.0 μsec
Termination	75 ohms
Video output	
Amplitude	Variable 0-4 volts
Pulse Width	0.7 $\pm$ 0.2 μsec
Termination	75 ohms
Rise Time	0.1 μsec

Table 1-3. Equipment Supplied

OFFICAL NOMENCLATURE	COMMON NAME	COMPONENT DESIGNATION	PART NO.	QTY	DESCRIPTION
Test Set, Video Signal Processor AN/TPM-32	Test Set		374571-1	1	
Combination Case	Case		386507-1	1	Contains cable assemblies, card extractor and manual
Electronic Assembly, Video Signal Processor Test Set			386041	1	Houses the electronics of test set
Card Extractor	Card Extractor		385546	1	Permits removal of circuit cards
Memory Cable Assembly	Cable Assembly		387170-1	1	Interconnection cable
Transfer Buffer Cable Assembly	Cable Assembly		387169-1	1	Interconnection cable

Table 1-3. Equipment Supplied (Cont)

OFFICIAL NOMENCLATURE	COMMON NAME	COMPONENT DESIGNATION	PART NO.	QTY	DESCRIPTION
Test Set Power Cable Assembly	Cable Assembly		387167-1	1	Interconnection cable
VSP Power Cable Assembly	Cable Assembly		387168-1	1	Interconnection cable
Coax Cable Assembly	Cable Assembly		387165-1	4	Interconnection cable
Test Lead Plug Assembly	Test Lead		387585-1	3	Used to hook up external test equipment.

1-11. EQUIPMENT REQUIRED BUT NOT SUPPLIED.

1-12. Equipment that is required for service and installation of the test set but which is not supplied with it is given in table 1-4.

Table 1-4. Equipment Required But Not Supplied

NAME	FEDERAL STOCK NUMBER	MODEL NO.	ALTERNATE
Pulse Generator	6625 113 1242	SG-816	Hewlet Packard, 8005A or Data Pulse No. 102
Multimeter	6625 724-8582	AN/PSM-6	Simpson, Model No. 260 or AN/USM 311
Oscilloscope	6625 892-5251	AN/USM-281	Tektronix, Type 454 Model 163D
Test Set, Patch Cable Assembly		387244-1	
Test Set, Patch Cable Assembly		387247-1	

CHAPTER 2

INSTALLATION

2-1. INTRODUCTION. This chapter contains installation information for the Video Signal Processor Test Set, AN/TPM-32. Section I provides the data required for effective installation planning. Section II gives logistics data. Section III contains the installation procedures, and includes references to tests required to make the test set operational. Section IV provides the procedures to be followed when reshipping the test set.

SECTION I

INSTALLATION PLANNING

2-2. LOCATION.

2-3. The test set can be used as a stand alone unit installed in the combination case in which it is received or can be removed from its combination case and installed in an equipment rack. In either case, the location of the test set must be chosen to permit all interconnecting cable assemblies to be connected between the VSP (Video Signal Processor) and the test set without introducing any strain or tension on the cables. Access to an electrical outlet is required to supply power to the test set.

2-4. ENVIRONMENTAL CONSIDERATION.

2-5. Refer to the environmental conditions specified in table 1-2 of Chapter 1.

2-6. POWER REQUIREMENTS.

2-7. The test set requires input supply of 105-132 volts ac, single phase, at 45 to 65 Hz or 380 to 420 Hz. The test set requires a total of 150 watts of power maximum.

2-8. SPECIAL TOOLS REQUIRED.

2-9. No special tools are required to install the test set either as a stand alone unit or as a rack mounted unit. A screwdriver is needed to open the inner lid inside the combination case cover to gain access to the cable assemblies, card extractor, and technical manual.

SECTION II

LOGISTICS

2-10. RECEIVING DATA.

2-11. Refer to shipping container contents in table 2-1 and to equipment supplied listed in table 1-1 of Chapter 1 to verify that all the proper items have been received.

2-12. UNPACKING.

2-13. Remove test set from shipping carton and save all packing material and packing carton for future shipment or storage.

2-14. INSPECTION.

2-15. No special inspection instructions are required, however a general visual check of the overall unit is recommended.

2-16. TRANSPORTABILITY.

2-17. No special transportability requirements are needed for the test set. Two men can adequately transport the test set while in its combination case by using the handles located on the side of the combination case.

Table 2-1. Shipping Container Contents

QTY.	DESCRIPTION	PART NO.
1	Electronic Assembly, Video Signal Processor Test Set	386041-1
1	Combination Case	386507-1
4	Cable Assembly	387165-1
1	Cable Assembly	387167-1
1	Cable Assembly	387168-1
1	Cable Assembly	387169-1
1	Cable Assembly	387170-1
3	Plug Assembly, Test Lead	387585-1
1	Extractor, card	385546-1

SECTION III

INSTALLATION PROCEDURES

2-18. GENERAL.

2-19. The test set is designed for use as a stand alone unit housed in its outer case or as a rack mounted unit removed from its outer case. Perform the following installation procedures applicable to how the test set is to be used.

2-20. GENERAL INSTALLATION INSTRUCTIONS.

2-21. FOR USE AS A STAND ALONE UNIT (UNMOUNTED). To install the test set as a stand alone unit, proceed as follows:

a. Place the test set so that the feet of the combination case rest on the ground.

NOTE

Before performing the next step, the PRESSURE EQUALIZER valve on the body of the combination case must be turned fully counterclockwise. This equalizes the air pressure inside the case with outside air pressure.

b. Disconnect the cover of the combination case from the outer case by releasing the hold down clamps.

NOTE

Observe cover position on the outer case. If cover is installed differently from the way it was removed, the attaching clamps cannot be connected.

c. Remove cover from outer case and place to one side.

d. Open the inner lid inside the cover by removing the captive screws. Refer to table 2-1 to verify contents.

e. Loosen the eight captive screws on the front panel of the test set and slide test set out of the outer case along the internal guide rails.

f. Perform the performance tests and fault isolation instructions given in chapter 5 to bring the test set to operational status.

g. Install test set into its combination case.

2-22. FOR USE AS A RACK MOUNTED UNIT. To install the test set as a rack mounted unit, proceed as follows:

a. Place the test set with the feet of the combination case resting on the ground.

NOTE

Before performing the next step, the PRESSURE EQUALIZER valve on the body of the combination case must be turned fully counterclockwise. This equalizes air pressure inside case with outside air pressure.

b. Disconnect the cover of the combination case from the outer case by releasing the hold down clamps.

NOTE

Observe cover position on the outer case. If cover is installed differently from the way it is removed, the attaching clamps cannot be connected.

c. Remove cover from outer case and set to one side.

d. Open the inner lid inside of cover by removing the captive screws. Refer to table 2-1 to verify contents.

e. Loosen the eight captive screws on the front panel of the test set and slide the test set out of the outer case along the internal guide rails.

f. Mount test set onto the equipment rack and secure in place.

g. Perform the performance tests and fault isolation instructions given in chapter 5 to bring the test set to operational status.

SECTION IV

PREPARATION FOR RESHIPMENT

2-23. For reshipment use the shipping carton held in storage or ship test set in its combination case. The cover of the combination case attaches to the outer case in only one way. If cover cannot be locked to case rotate cover 180°.

NOTE

Ensure that all circuit cards are properly seated in their connector receptacles before shipping.

CHAPTER 3

OPERATION

3-1. INTRODUCTION. This chapter contains instructions and procedures needed to operate the Video Signal Processor Test Set, AN/TPM-32. Section I contains illustrations of the test set controls and indicators and tables describing the functions of each. Section II gives the starting, operating and stopping procedures for the test set.

SECTION I

CONTROLS AND INDICATORS

3-2. The controls, indicators and connectors of the test set are shown in figure 3-1 and their functions are given in table 3-1. The rear panel controls and connectors of the test set are shown in figure 3-2 and their functions are given in table 3-2.

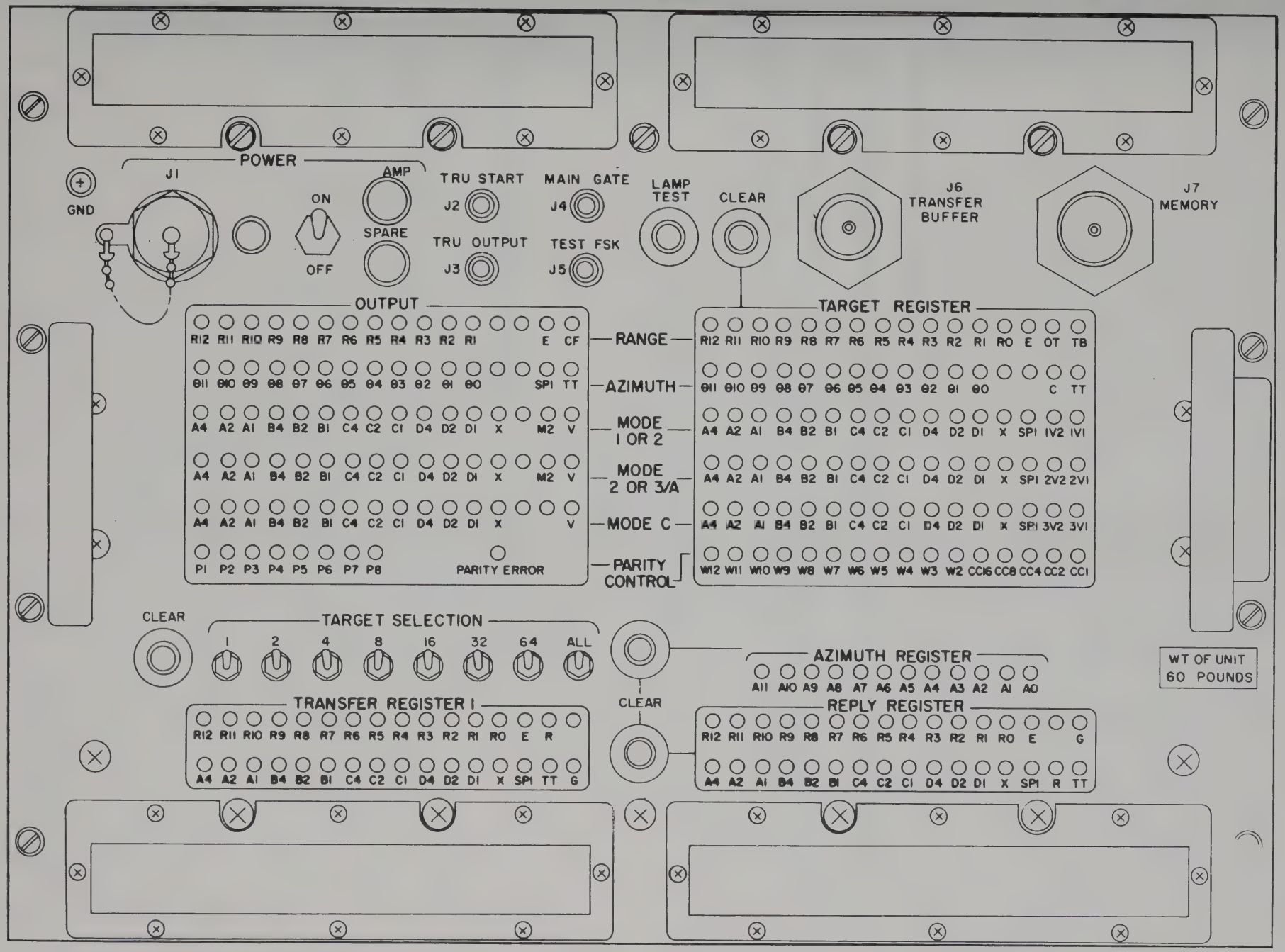

POWER
J1
GND
ON
OFF
AMP
SPARE
TRU START
J2
TRU OUTPUT
J3
MAIN GATE
J4
TEST FSK
J5
LAMP TEST
CLEAR
J6
TRANSFER BUFFER
J7
MEMORY
OUTPUT
RI2 RII RIO R9 R8 R7 R6 R5 R4 R3 R2 RI E CF
θII θIO θ9 θ8 θ7 θ6 θ5 θ4 θ3 θ2 θI θO SPI TT
A4 A2 AI B4 B2 BI C4 C2 CI D4 D2 DI X M2 V
A4 A2 AI B4 B2 BI C4 C2 CI D4 D2 DI X M2 V
A4 A2 AI B4 B2 BI C4 C2 CI D4 D2 DI X V
PI P2 P3 P4 P5 P6 P7 P8
PARITY ERROR
RANGE
AZIMUTH
MODE 1 OR 2
MODE 2 OR 3/A
MODE C
PARITY CONTROL
TARGET REGISTER
RI2 RII RIO R9 R8 R7 R6 R5 R4 R3 R2 RI RO E OT TB
θII θIO θ9 θ8 θ7 θ6 θ5 θ4 θ3 θ2 θI θO C TT
A4 A2 AI B4 B2 BI C4 C2 CI D4 D2 DI X SPI IV2 IVI
A4 A2 AI B4 B2 BI C4 C2 CI D4 D2 DI X SPI 2V2 2VI
A4 A2 AI B4 B2 BI C4 C2 CI D4 D2 DI X SPI 3V2 3VI
W12 WII WIO W9 W8 W7 W6 W5 W4 W3 W2 CC16 CC8 CC4 CC2 CCI
CLEAR
TARGET SELECTION
1 2 4 8 16 32 64 ALL
TRANSFER REGISTER I
RI2 RII RIO R9 R8 R7 R6 R5 R4 R3 R2 RI RO E R
A4 A2 AI B4 B2 BI C4 C2 CI D4 D2 DI X SPI TT G
CLEAR
AZIMUTH REGISTER
AII AIO A9 A8 A7 A6 A5 A4 A3 A2 AI AO
REPLY REGISTER
RI2 RII RIO R9 R8 R7 R6 R5 R4 R3 R2 RI RO E G
A4 A2 AI B4 B2 BI C4 C2 CI D4 D2 DI X SPI R TT
WT OF UNIT
60 POUNDS

FIGURE 3-1. TEST SET, VIDEO SIGNAL PROCESSOR AN/TPM-32 FRONT PANEL CONTROLS, INDICATORS AND CONNECTORS

Table 3-1. Video Signal Processor AN/TPM-32 Test Set Front Panel Controls, Indicators, and Connectors

NAME	REFERENCE DESIGNATION	FUNCTION
POWER ON/OFF switch	S1	Provide 115 Vac to test set.
LAMP TEST pushbutton	S2	When depressed, provides power to all front panel indicators except DS1 (POWER ON indicator)
CLEAR pushbutton	S3	When depressed, clears target register of unit under test.
CLEAR pushbutton	S4	When depressed, clears transfer register of unit under test.
TARGET SELECTION switches	S5-S11	Select target data word from TRU OUTPUT of unit under test.
TARGET SELECTION ALL switch	S12	In up position, all TRU OUTPUT data of unit under test are displayed by OUTPUT indicators on front panel.

Table 3-1. Video Signal Processor AN/TPM-32 Test Set Front Panel Controls, Indicators, and Connectors (Cont)

NAME	REFERENCE DESIGNATION	FUNCTION
CLEAR pushbutton	S13	When depressed, clears azimuth register of unit under test.
CLEAR pushbutton	S15	When depressed, clears reply register of unit under test.
POWER indicator	DS1	Lights to indicate power is supplied to test set.
OUTPUT indicators	A1DS1-A1DS32 A2DS1-A2DS32 A3DS1-A3DS24	Display TRU OUTPUT data word (selected by switches S5-S13) of unit under test.
	A3DS29	Lights to indicate incorrect parity in TRU OUTPUT word.
TRANSFER REGISTER indicators	A4DS1-A4DS32	Display contents of transfer register of unit under test for longest range target being processed.

Table 3-1. Video Signal Processor AN/TPM-32 Test Set Front Panel Controls, Indicators, and Connectors (Cont)

NAME	REFERENCE DESIGNATION	FUNCTION
TARGET REGISTER	A5DS1-A5DS32 A6DS1-A6DS32 A7DS1-A7DS32	Display contents of target register of unit under test for shortest range target being processed
AZIMUTH REGISTER indicator	A8DS1-A8DS32	Displays contents of azimuth register of unit under test.
REPLY REGISTER indicator	A9DS1-A9DS32	Displays contents of reply register of unit under test for shortest range being processed.
POWER connector	J1	Connects 115 Vac to test set when S14 is in J1 position.
TRU START connector	J2	Provides test point for monitoring TRU start signals from unit under test or for triggering oscilloscope.

Table 3-1. Video Signal Processor AN/TPM-32 Test Set Front Panel Controls, Indicators, and Connectors (Cont)

NAME	REFERENCE DESIGNATION	FUNCTION
TRU OUTPUT connector	J3	Provides test point for monitoring TRU OUTPUT signals from unit under test or for triggering oscilloscope.
MAIN GATE connector	J4	Provides test point for monitoring main gate signals from unit under test or for triggering oscilloscope.
TEST FSK connector	J5	Provides a connection for inserting a TEST FSK signal into test set, or a test point for monitoring FSK output of unit under test. CAUTION Disconnect J6 before inserting TEST FSK signal into J5.

Table 3-1. Video Signal Processor, AN/TPM Test Set Front Panel Controls, Indicators, and Connectors (Cont)

NAME	REFERENCE DESIGNATION	FUNCTION
TRANSFER BUFFER connector	J6	Connects signals from unit under test to test set.
MEMORY connector	J7	Connects signals from unit under test to test set, and manual clear commands from test set to the unit under test.
AMP fuse	F1	Protects test set from damage caused by short circuits or overloads
SPARE fuse	F2	

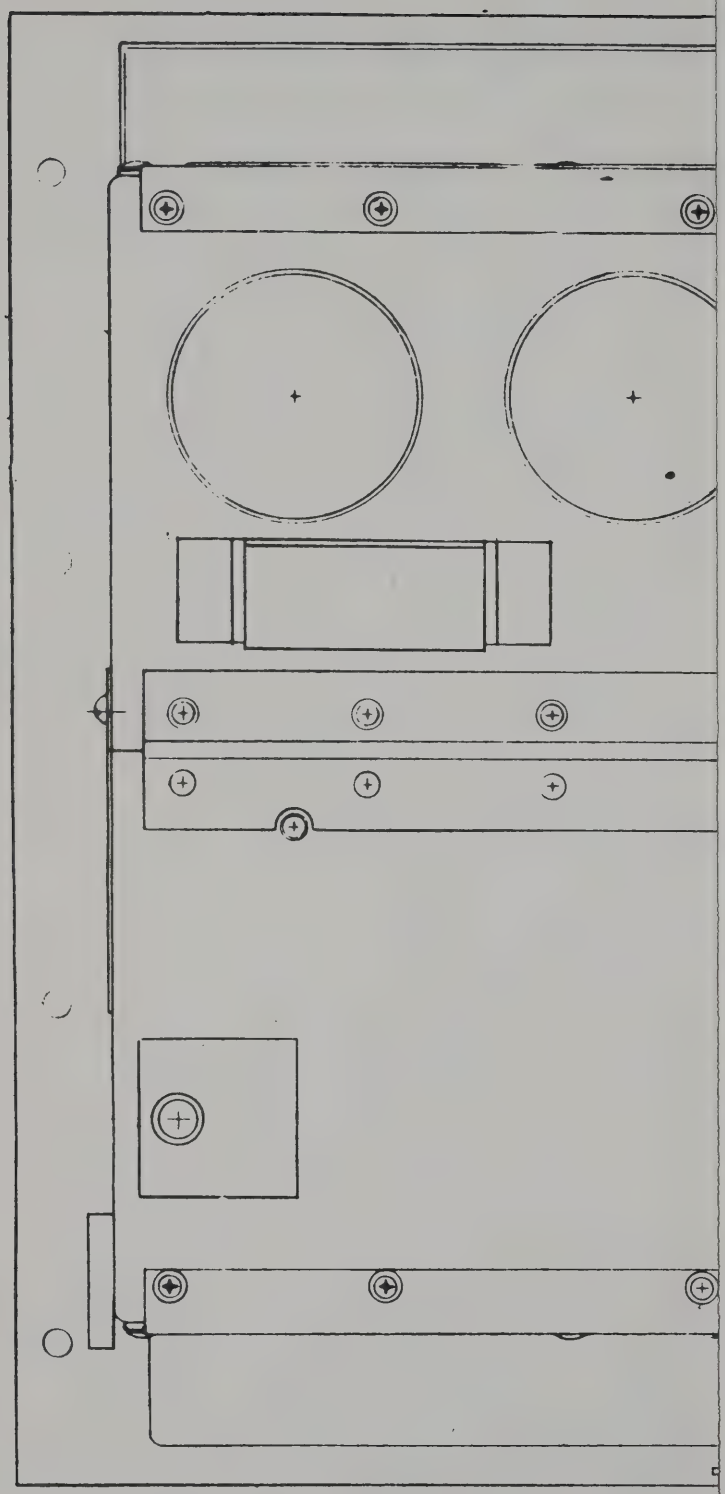


FIGURE 3-2. TEST SET, VIDEO SIGNAL PROCESS
INDICATORS AND CO

Table 3-2. Video Signal Processor, AN/TPM-32, Test Set Rear Panel Controls and Connectors

NAME	REFERENCE DESIGNATORS	FUNCTION
POWER INPUT SELECTION switch	S14	Selects either J1 on front panel or J8 for power input to test set.
POWER connector	J8	Connects 115 Vac to test set when S14 is in J8 position.

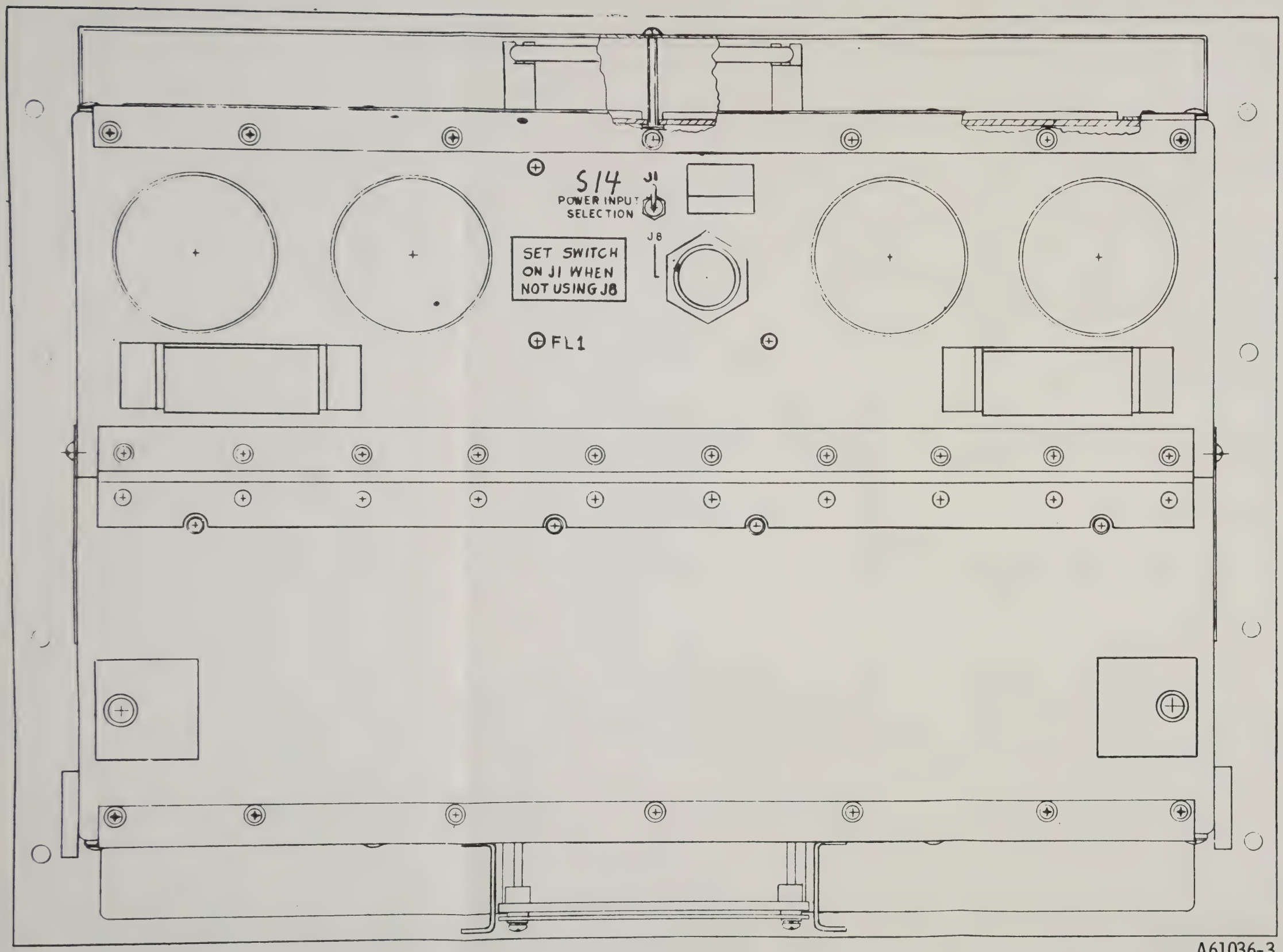


FIGURE 3-2. TEST SET, VIDEO SIGNAL PROCESSOR AN/TPM-32 REAR PANEL CONTROLS INDICATORS AND CONNECTORS

Table 3-2. Video Signal Processor, AN/TPM-32, Test Set Rear Panel Controls and Connectors

NAME	REFERENCE DESIGNATORS	FUNCTION
POWER INPUT SELECTION switch	S14	Selects either J1 on front panel or J8 for power input to test set.
POWER connector	J8	Connects 115 Vac to test set when S14 is in J8 position.

SECTION II

OPERATION PROCEDURES

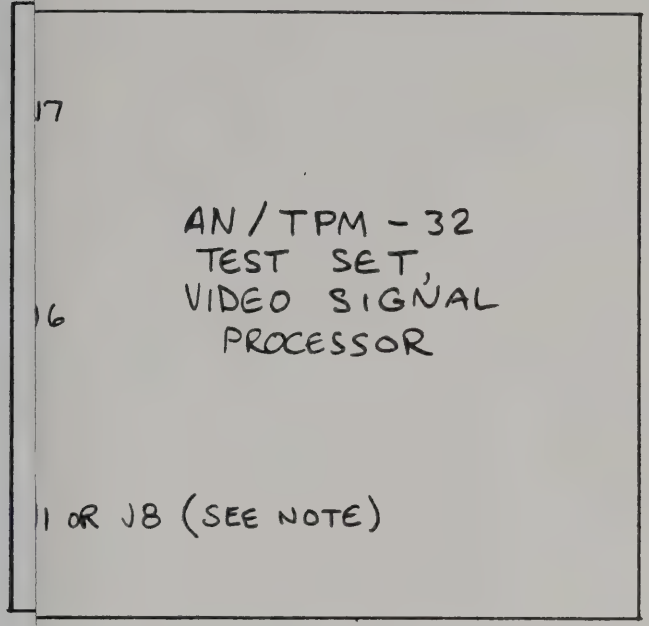
3-3. STARTING PROCEDURE.

3-4. The starting procedure for the test set consists of interconnecting the test set to the Video Processor, CP-1045/T as shown in figure 3-3.

3-5. OPERATING PROCEDURE.

3-6. The operating procedure for the test set is used to test the Video Processor, CP-1045/T. For these instructions refer to the Video Processor, CP-1045/T service manual (T.O. 31P4-2T-33).

3-7. STOPPING PROCEDURE (NOT APPLICABLE).



IN ITS COMBINATION CASE,
BLY (PART NO. 387167-1)
ONT PANEL CONNECTOR J1
SELECTION SWITCH ON THE
IN THE J1 POSITION. WHEN
NTED, THE POWER CABLE
TO THE REAR PANEL CONNECTOR,
UT SELECTION SWITCH IS
ITION.

A61036-4

45/T PERFORMANCE TEST SETUP DIAGRAM

SECTION II

OPERATION PROCEDURES

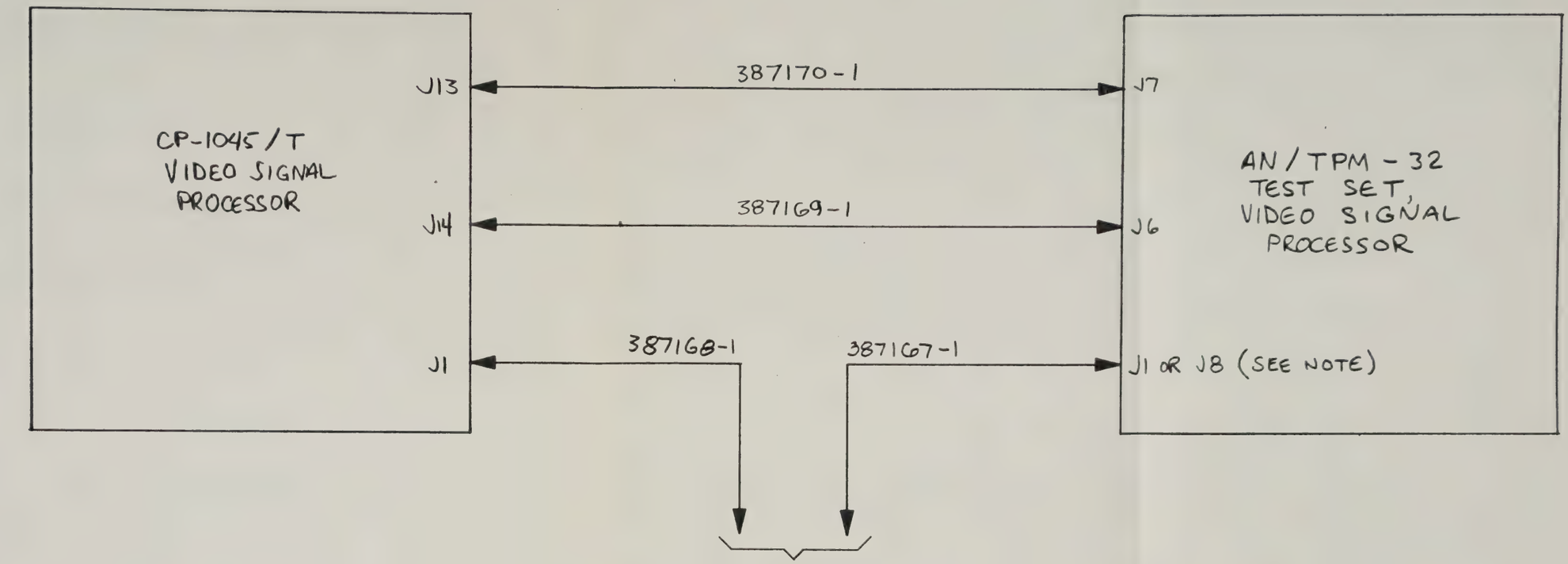
3-3. STARTING PROCEDURE.

3-4. The starting procedure for the test set consists of interconnecting the test set to the Video Processor, CP-1045/T as shown in figure 3-3.

3-5. OPERATING PROCEDURE.

3-6. The operating procedure for the test set is used to test the Video Processor, CP-1045/T. For these instructions refer to the Video Processor, CP-1045/T service manual (T.O. 31P4-2T-33).

3-7. STOPPING PROCEDURE (NOT APPLICABLE).



NOTE:
WHEN TEST SET IS USED IN ITS COMBINATION CASE, THE POWER CABLE ASSEMBLY (PART NO. 387167-1) IS CONNECTED TO THE FRONT PANEL CONNECTOR J1 AND THE POWER INPUT SELECTION SWITCH ON THE REAR PANEL IS PLACED IN THE J1 POSITION. WHEN TEST SET IS RACK MOUNTED, THE POWER CABLE ASSEMBLY IS CONNECTED TO THE REAR PANEL CONNECTOR, J8, AND THE POWER INPUT SELECTION SWITCH IS PLACED IN THE J8 POSITION.

A61036-4

FIGURE 3-3. VIDEO SIGNAL PROCESSOR, CP-1045/T PERFORMANCE TEST SETUP DIAGRAM

SECTION III

EMERGENCY OPERATION

NOT APPLICABLE

CHAPTER 4

PRINCIPLES OF OPERATION

4-1. INTRODUCTION. This chapter provides the principles of operation of Test Set, Video Signal Processor AN/TPM-32. Section I describes the AN/TPM-32 on an overall block diagram level, relating the various functional circuit groups to each other and to the Processor, Video Signal CP-1045/T of Interrogator Set AN/TPX-42A(V). Section II provides detailed block diagram discussions and circuit descriptions of the components with reference to T.O. 33D7-24-13-3 for overall and printed circuit card schematic diagrams. Section III is not applicable. Refer to T.O. 31-1-141 for basic circuits theory of operation.

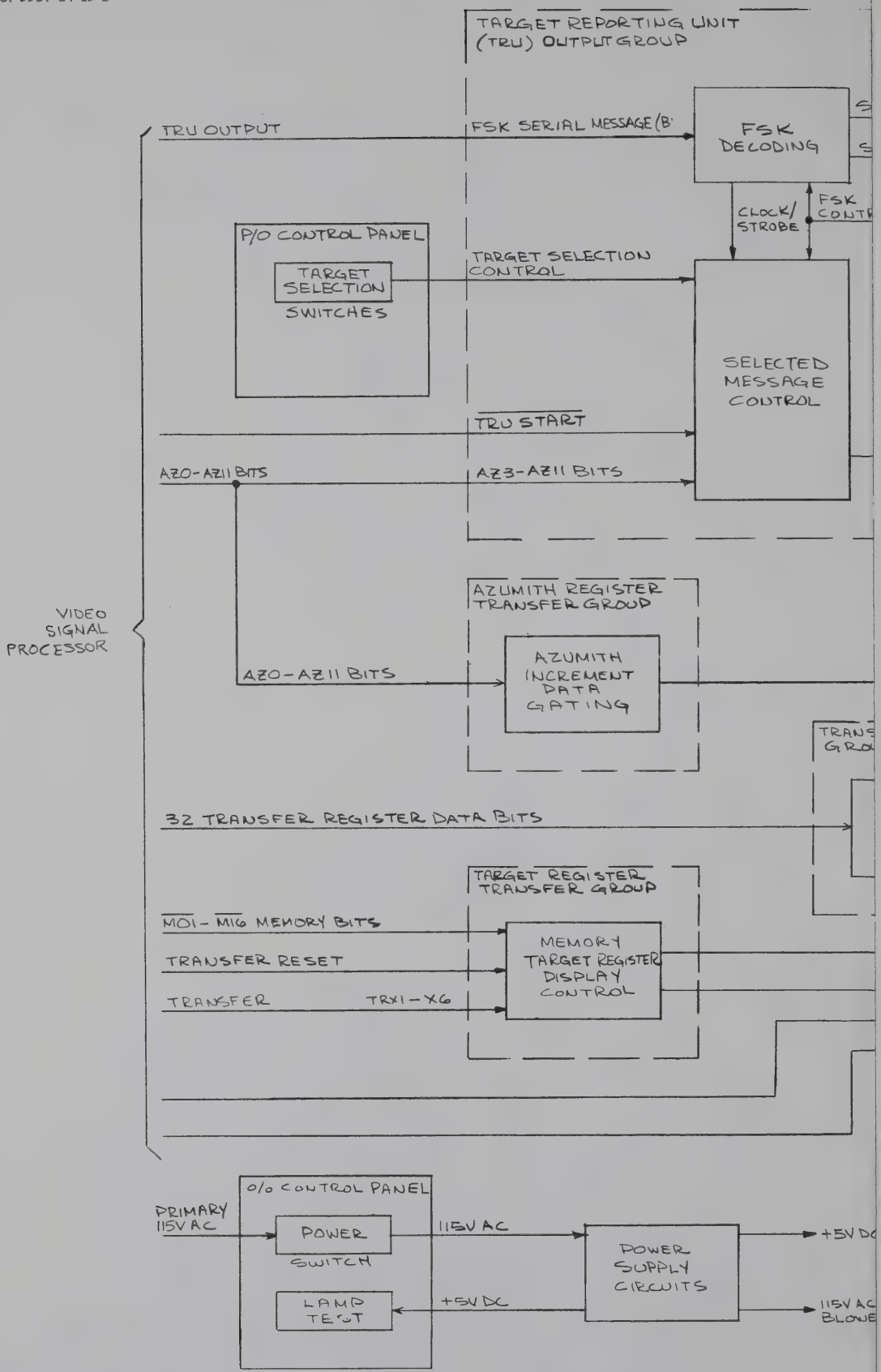


FIGURE 4-1. TEST SET, VIDEO SIGNAL PROCESSOR AN/TPM-32 OVERALL BLOCK DIAGRAM

SECTION I

FUNCTIONAL SYSTEM OPERATION

4-2. OVERALL FUNCTIONAL BLOCK DIAGRAM DISCUSSION.

4-3. The test set consists of power distribution circuits, manual clearing and monitoring circuits and five functional groups (figure 4-1): target reporting unit (TRU) output, azimuth register, transfer register, target register, and reply register.

4-4. The TRU output group contains FSK decoding, FSK data register, selected message control, and message parity checking circuits. These circuits perform two functions: to select, for display, one target-reporting test message from the video signal processor, and to determine if any parity error exists in the selected test message. A total of 120 target reporting test messages can be monitored by the test set. The number of the test message selected is determined by the setting of applicable control panel TARGET SELECTION switches. Target selection control signals from the control panel are then applied to the selected message control circuits to establish the number of test message inputs (represented by $\overline{\text{TRU START}}$ input signals) that must be counted until the selected test message is reached. (The $\overline{\text{TRU START}}$ inputs are synced to the start of each FSK-coded message.) After the selected FSK-coded message is received, the selected message control circuits count the number of data and parity bits serially inserted into the FSK decoding circuits. The target selection function of the selected

message control circuits is controlled by the nine most significant azimuth position bits from the video signal processor and the bit counting function of the circuits is controlled by clock/strobe and FSK control (sync) signals from the FSK decoding circuits. The selected message control circuits provide parity strobe and FSK control (end of message) signals. The parity strobe signals are developed at every eighth bit of the input message for use by message parity checker circuits in detection of any parity error. The end of message (EOM) control signals are developed at the end of serial message for use by message parity checker and selected message control circuits. The FSK decoding circuits decode the FSK format of the selected test message (received on the $\overline{\text{TRU OUTPUT}}$ line) and provide a serial data message in conventional logic level format for input to the message data register circuits. Also provided are clock/strobe and FSK control sync signals to control the counting functions of the selected message control circuits. The message data register circuits clock in the serial data from the FSK decoding circuits and provide parallel digital data output in the form of five 16-bit words and eight parity bits for display by the OUTPUT lamps on the test set control panel. The message parity checker, using parallel digital data output of the FSK data register circuits, the FSK control (sync and EOM) signals, and the parity strobe signal, provides a parity error signal output that lights PARITY ERROR lamp in OUTPUT section of control panel when a parity error is detected.

4-5. The azimuth register functional group contains azimuth position data gating circuits that gate through the incoming azimuth position bits AZ0 to AZ11 from the video signal processor for display on the AZIMUTH REGISTER lamps of the test set control panel.

4-6. The transfer register group contains circuits that permit 32 transfer register data bits from the video signal processor to be displayed on the TRANSFER REGISTER lamps of the test set control panel.

4-7. The target register group contains memory target register control circuits that demultiplex the incoming 16 memory data bits through timing of six input transfer strobes (TRX1-TRX6). The resultant six 16-bit words are then displayed by the TARGET REGISTER lamps on the test set control panel. A reset input from the video signal processor clears the memory target control circuits for the next group of memory target data bits.

4-8. The reply register group contains memory reply register control circuits that demultiplex the 16 memory data bits, inputted from the video signal processor through the memory target control circuits, by means of timing of two input reply strobes (RRX1 and RRX2). The resultant two 16-bit words are then displayed by the REPLY REGISTER lamps on the test set control panel. A reply reset input from the video signal processor clears the memory reply control circuits for the next group of memory reply data bits.

4-9. When primary 115 volts ac is applied, through POWER switch of the control panel, the power supply circuits provide operating +5 volts dc for the digital circuits in the functional groups of the test set and 115 volts ac for operation of a blower to cool the test set. The power supply circuits also provide +5 volts dc through control panel LAMP TEST pushbutton switch for self-testing of the control panel display lamps.

4-10. Manual clearing of the target register, azimuth register, reply register, and transfer register within the video signal processor is provided by a corresponding CLEAR pushbutton on the test set control panel. Front panel connectors permit monitoring, by an external test oscilloscope, of the TRU START, TRU OUTPUT, and MAIN GATE inputs from the video signal processor. Test FSK-coded type serial messages from external equipment other than the video signal processor can be inserted into the test set at a front panel connector.

SECTION II

FUNCTIONAL OPERATION OF ELECTRONIC CIRCUITS

4-11. TRU OUTPUT FUNCTIONAL GROUP.

4-12. The target reporting unit (TRU) outputs functional group consists of FSK decoding circuits, selected message control, FSK data register, and the message parity checker. The TRU output functional group converts a selected FSK-coded serial message input from the video signal processor into a conventional logic level serial message for display on the OUTPUT display lamps of the control panel. The FSK-coded message input can also be obtained from any suitable external equipment other than the video signal processor. The TRU output group also develops necessary clock, strobe, sync, and other signals to control the functioning of all circuits within the functional group.

4-13. FSK DECODING CIRCUITS BLOCK DIAGRAM DISCUSSION. The FSK decoding circuits consist of a FSK clock, a FSK decoder (receiver), and shift clock gates (figure 4-2). The FSK clock provides a train of 5.18 MHz square wave pulses, that are applied to the FSK receiver as the operating clock input. The FSK receiver then develops internal clocking signals that permit the circuitry to convert the FSK-coded format of the selected input serial message from the video signal processor into a serial message of conventional logic level format. The output serial data is applied from the FSK decoding circuits to the message data register of the TRU output functional group for eventual display on the test set control panel. The shift clock gates provide the shift

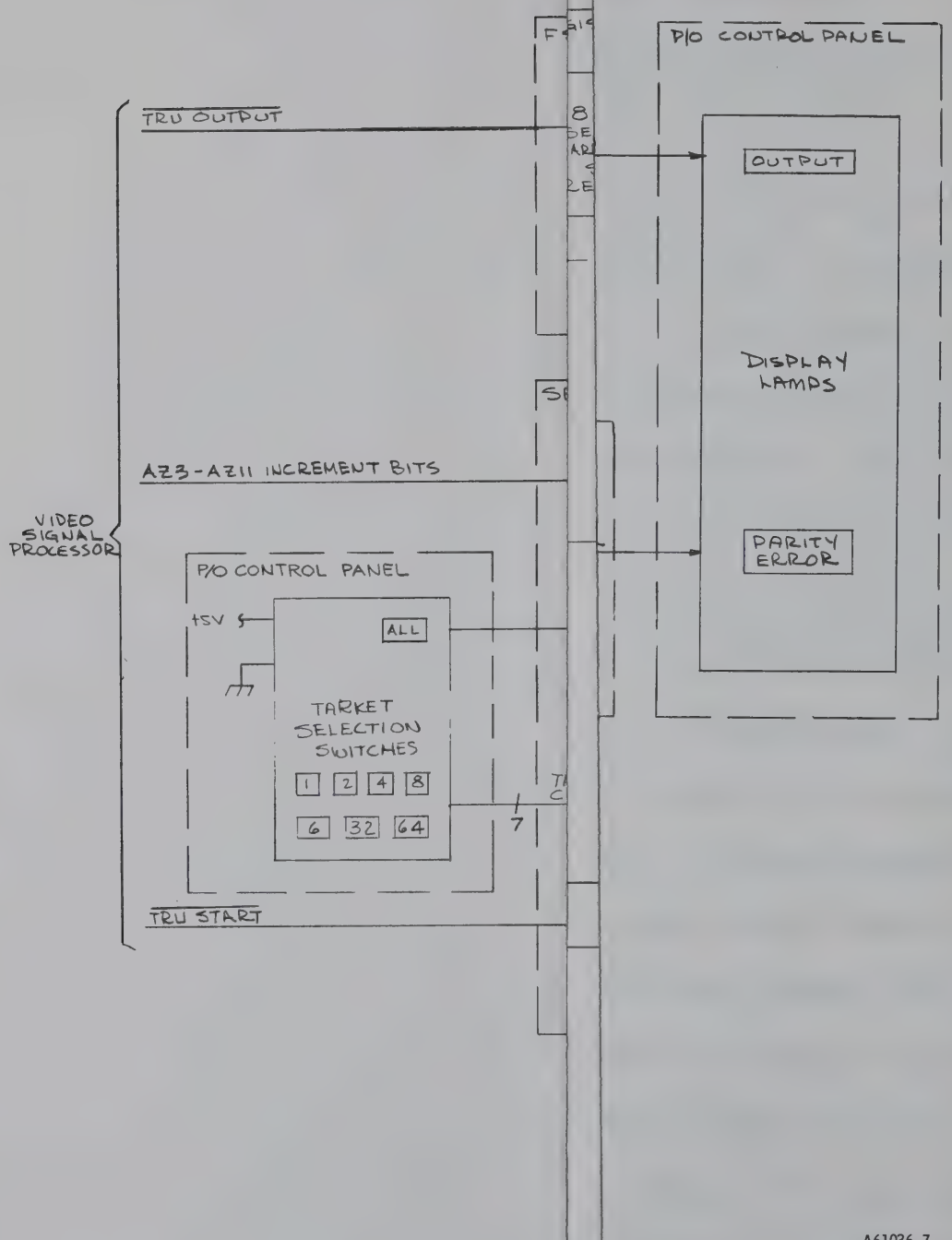
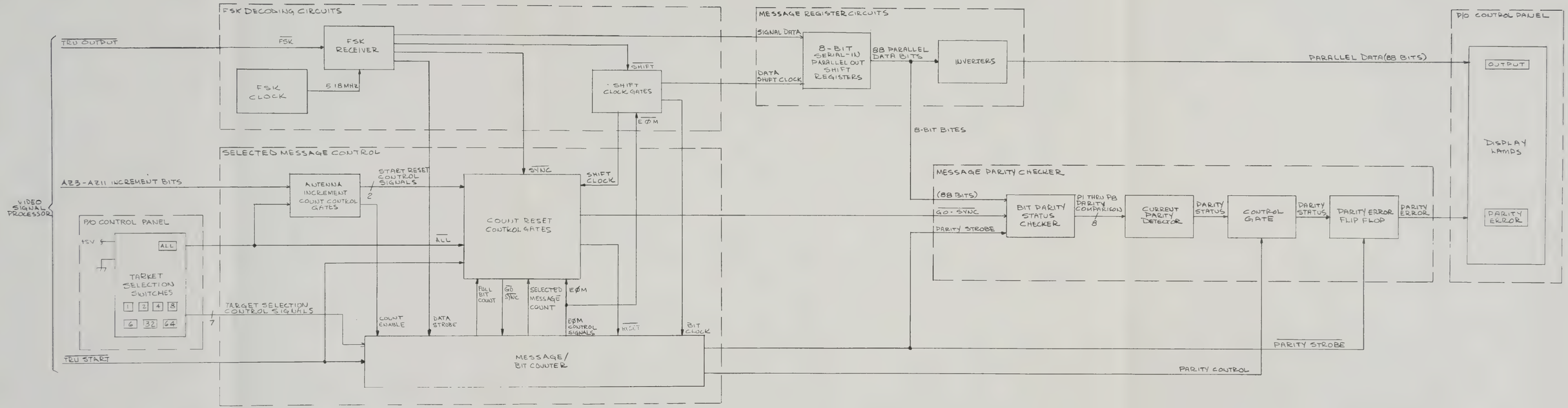


FIGURE 4-2. TARGET REPORTING UNIT OUTPUT CIRCUITS, BLOCK DI

clocks used for clocking functions performed by the FSK data register and selected message control circuits.

4-14. The FSK receiver develops three control and clock signals: $\overline{\text{SYNC}}$, $\overline{\text{SHIFT}}$, and DATA STROBE. The $\overline{\text{SYNC}}$ signal is a narrow pulse that appears once every data message to indicate the start of data reception. The $\overline{\text{SHIFT}}$ and DATA STROBE signals are each a train of narrow pulses occurring, except at the sync start, once every data bit period (42.5μ sec) and each serves as a clocking signal representing a bit period. The $\overline{\text{SYNC}}$ signal is applied to control the resetting operation of the selected message control circuits. The $\overline{\text{SHIFT}}$ signal is applied to the shift clock gates to be gated out as shift clocks for application to the selected message control circuits and message parity checker circuits of the TRU output functional group. The DATA STROBE signal is applied to the selected message control circuits for use in the generation of periodic parity strobe control signals (every 8th bit) needed by the message parity checker for parity comparison. The shift clock gates of the FSK decoding circuits receive an end of message ($\overline{\text{EOM}}$) signal from the selected message control circuits to inhibit the bit and data shift clock outputs of the gates. In this manner, the bit-counting function of the selected message control circuits and the data clocking of the FSK data registers are stopped at the end of the message.

4-15. FSK DECODING CIRCUIT ANALYSIS. The following paragraphs discuss the circuit analysis of the FSK clock, FSK receiver, and shift clock gates comprising the FSK decoding circuits. This discussion is supported by test set and circuit card schematic diagrams in T.O. 33D7-24-13-3.



A61036-7

FIGURE 4-2. TARGET REPORTING UNIT OUTPUT CIRCUITS, BLOCK DIAGRAM

clocks used for clocking functions performed by the FSK data register and selected message control circuits.

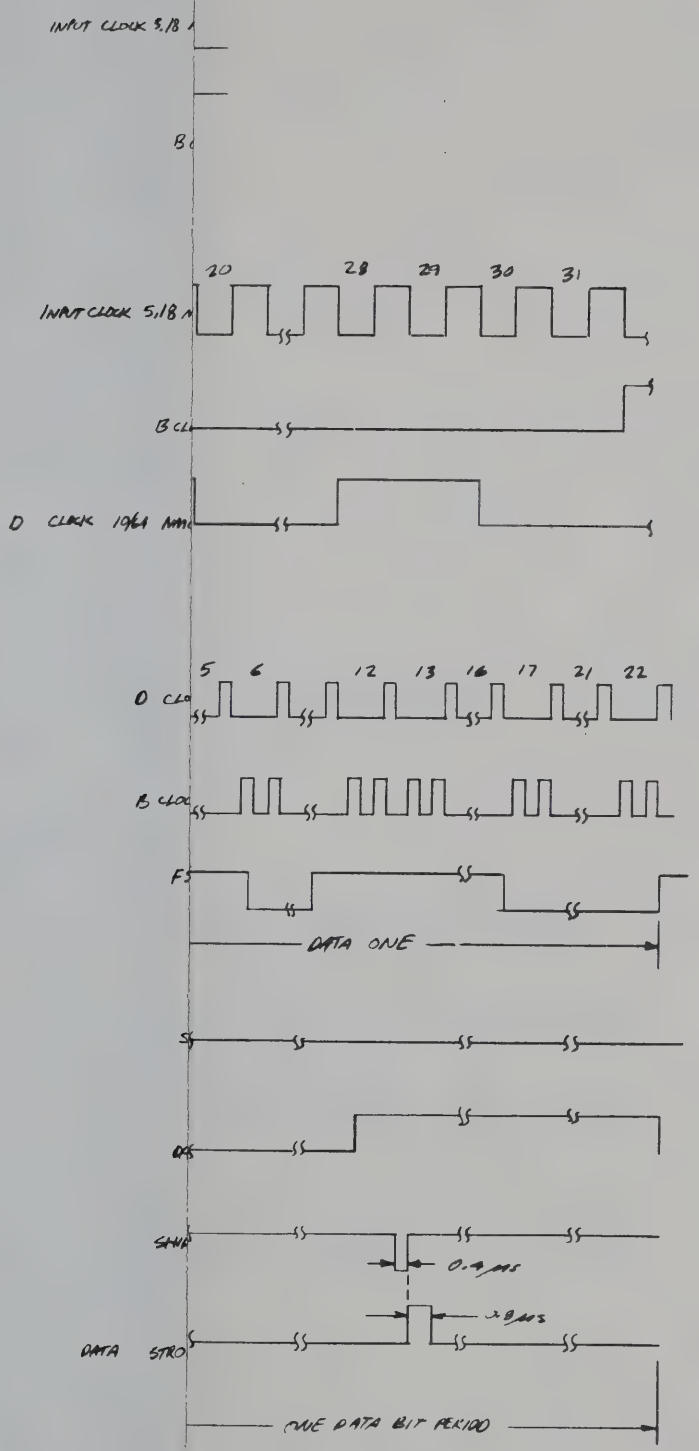
4-14. The FSK receiver develops three control and clock signals: $\overline{\text{SYNC}}$, $\overline{\text{SHIFT}}$, and DATA STROBE. The $\overline{\text{SYNC}}$ signal is a narrow pulse that appears once every data message to indicate the start of data reception. The $\overline{\text{SHIFT}}$ and DATA STROBE signals are each a train of narrow pulses occurring, except at the sync start, once every data bit period (42.5μ sec) and each serves as a clocking signal representing a bit period. The $\overline{\text{SYNC}}$ signal is applied to control the resetting operation of the selected message control circuits. The $\overline{\text{SHIFT}}$ signal is applied to the shift clock gates to be gated out as shift clocks for application to the selected message control circuits and message parity checker circuits of the TRU output functional group. The DATA STROBE signal is applied to the selected message control circuits for use in the generation of periodic parity strobe control signals (every 8th bit) needed by the message parity checker for parity comparison. The shift clock gates of the FSK decoding circuits receive an end of message ($\overline{\text{EOM}}$) signal from the selected message control circuits to inhibit the bit and data shift clock outputs of the gates. In this manner, the bit-counting function of the selected message control circuits and the data clocking of the FSK data registers are stopped at the end of the message.

4-15. FSK DECODING CIRCUIT ANALYSIS. The following paragraphs discuss the circuit analysis of the FSK clock, FSK receiver, and shift clock gates comprising the FSK decoding circuits. This discussion is supported by test set and circuit card schematic diagrams in T.O. 33D7-24-13-3.

4-16. FSK Clock. The FSK clock (refer to T.O. 33D7-24-13-3 for overall schematic diagram) consists of a crystal oscillator A301-Y1 and flip-flop A303-U3B. The crystal oscillator A301-Y1 provides a clock signal at a frequency of 10.356 MHz, which is used to toggle flip-flop A303-U3B. Flip-flop A303-U3B functions as a frequency halver and the resultant output at pin A303-38 is a clock frequency of 5.18 MHz, applied to pin A305-14 of the FSK receiver at the 10.356 MHZ input.

4-17. FSK Receiver. The FSK receiver consists entirely of FSK printed circuit card A305 (refer to T.O. 33D7-24-13-3 for circuit card schematic diagram). Timing sequence for all inputs and outputs of the FSK receiver is shown in figure 4-3. Inputs to the FSK receiver are the serial signal in FSK-coded format from the video signal processor and the 5.18 MHz clock from the FSK clock in the FSK decoding circuits. Outputs from the FSK receiver are the corresponding serial signal in logic level format, and three control signals: $\overline{\text{SYNC}}$, $\overline{\text{SHIFT}}$, and DATA STROBE.

4-18. The input selected message, consisting of a sync character and 88 data bits in FSK-coded format (figure 4-4), is applied to FSK receiver at pin A305-32 as the $\overline{\text{FSK}}$ input. The FSK receiver decodes and converts this FSK-coded input message and the resultant output serial test message, consisting of 88 corresponding data bits in conventional binary format, appears at output pin A305-30 as the DATA signal. The DATA signal is applied to pin A308-5 in the message data register circuits to be clocked into serial-in, parallel-out shift registers for eventual display on the test set control panel.



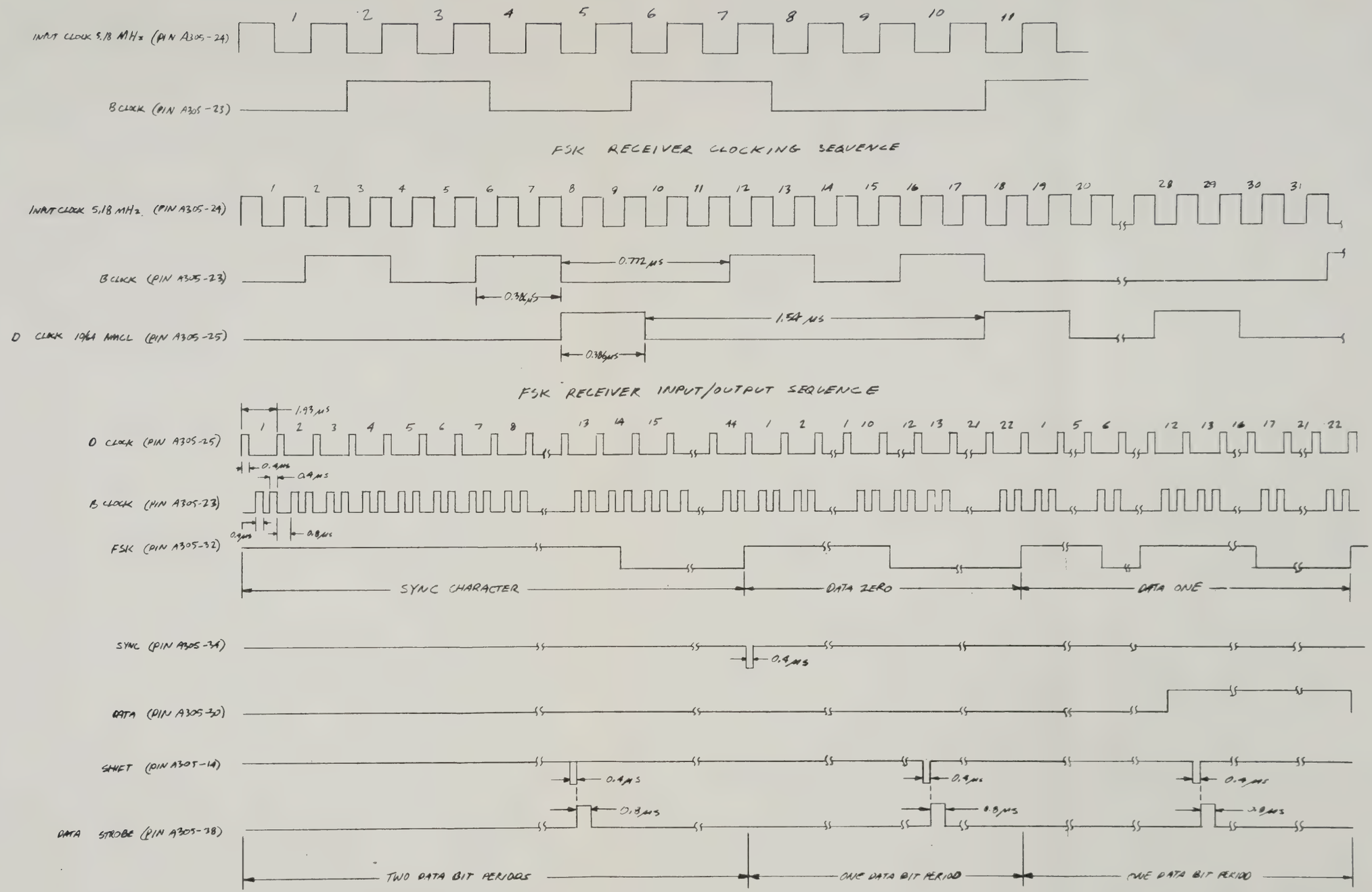
A61036-8

5K RECEIVER INPUT/OUTPUT AND CLOCK TIMING DIAGRAM

4-16. FSK Clock. The FSK clock (refer to T.O. 33D7-24-13-3 for overall schematic diagram) consists of a crystal oscillator A301-Y1 and flip-flop A303-U3B. The crystal oscillator A301-Y1 provides a clock signal at a frequency of 10.356 MHz, which is used to toggle flip-flop A303-U3B. Flip-flop A303-U3B functions as a frequency halver and the resultant output at pin A303-38 is a clock frequency of 5.18 MHz, applied to pin A305-14 of the FSK receiver at the 10.356 MHZ input.

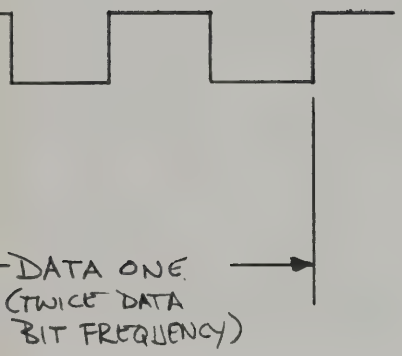
4-17. FSK Receiver. The FSK receiver consists entirely of FSK printed circuit card A305 (refer to T.O. 33D7-24-13-3 for circuit card schematic diagram). Timing sequence for all inputs and outputs of the FSK receiver is shown in figure 4-3. Inputs to the FSK receiver are the serial signal in FSK-coded format from the video signal processor and the 5.18 MHz clock from the FSK clock in the FSK decoding circuits. Outputs from the FSK receiver are the corresponding serial signal in logic level format, and three control signals: $\overline{\text{SYNC}}$, $\overline{\text{SHIFT}}$, and DATA STROBE.

4-18. The input selected message, consisting of a sync character and 88 data bits in FSK-coded format (figure 4-4), is applied to FSK receiver at pin A305-32 as the $\overline{\text{FSK}}$ input. The FSK receiver decodes and converts this FSK-coded input message and the resultant output serial test message, consisting of 88 corresponding data bits in conventional binary format, appears at output pin A305-30 as the DATA signal. The DATA signal is applied to pin A308-5 in the message data register circuits to be clocked into serial-in, parallel-out shift registers for eventual display on the test set control panel.


INPUT CLOCK 5.18 MHz (PIN A305-24)
1 2 3 4 5 6 7 8 9 10 11
B CLOCK (PIN A305-23)
FSK RECEIVER CLOCKING SEQUENCE
INPUT CLOCK 5.18 MHz (PIN A305-24)
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 28 29 30 31
B CLOCK (PIN A305-23)
0.772 µs
0.386 µs
D CLOCK 1/64 NRZCL (PIN A305-25)
1.54 µs
0.386 µs
FSK RECEIVER INPUT/OUTPUT SEQUENCE
D CLOCK (PIN A305-25)
1.93 µs
1 2 3 4 5 6 7 8 13 14 15 1 2 1 10 12 13 21 22 1 5 6 12 13 16 17 21 22
0.4 µs
0.4 µs
B CLOCK (PIN A305-23)
FSK (PIN A305-32)
0.4 µs
0.8 µs
SYNC CHARACTER
DATA ZERO
DATA ONE
SYNC (PIN A305-34)
0.4 µs
DATA (PIN A305-30)
SHIFT (PIN A305-14)
0.4 µs
0.4 µs
0.4 µs
DATA STROBE (PIN A305-38)
0.8 µs
0.8 µs
0.8 µs
TWO DATA BIT PERIODS
ONE DATA BIT PERIOD
ONE DATA BIT PERIOD

A61036-8

FIGURE 4-3. FSK RECEIVER INPUT/OUTPUT AND CLOCK TIMING DIAGRAM

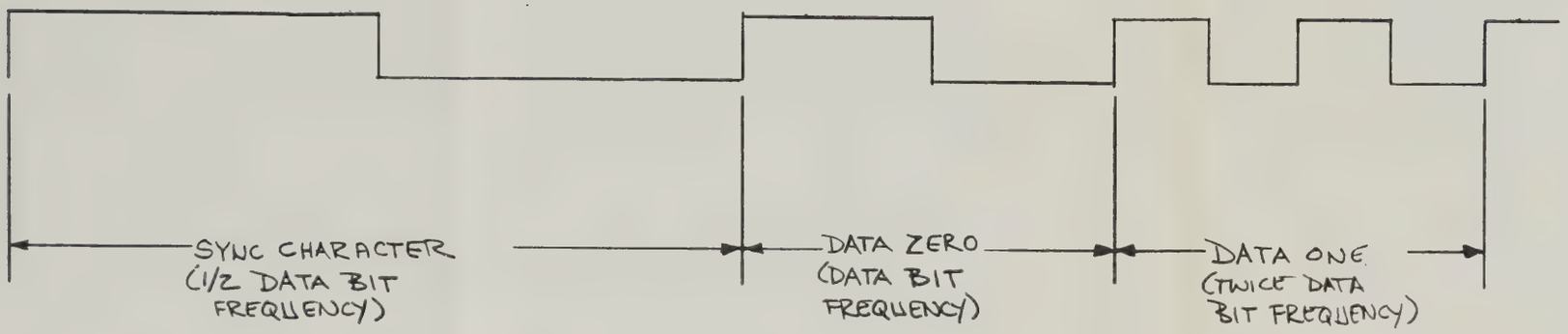


A61036-9

4-19. The FSK receiver is clocked by a 5.18 MHz clock from the FSK clock circuits. (The 5.18 MHz clock is equivalent to 1/64 nautical mile (nm) or about 0.2 μsec clock.) Two clocks are then internally generated by the FSK receiver A305. One clock, known as the D or 10/64 nm clock, appears at pin A305-25. The D clock is jumpered back to pins A305-40 and A305-26 for use as the DATA clock and COUNT clock, respectively. The other internally generated clock is known as the B clock and appears at pin A305-23. The B clock is jumpered back to pin A305-21 as the DATA STROKE clock.

4-20. After the end of sync character period in the input test message, a $\overline{\text{SYNC}}$ signal appears at output pin A305-34 of the FSK receiver and is applied to pin A307-25 of the count reset control gates and to pin A304-17 of the message/bit counter in the selected message control circuit. A SHIFT signal is generated once every data bit period, or approximately 42.5 μsec except when a sync signal is present. The train of $\overline{\text{SHIFT}}$ pulses appears at output pin A305-14 of the FSK receiver and is applied to pin A306-21 of the shift clock gates. In every data bit period, a DATA STROBE signal is generated immediately after the $\overline{\text{SHIFT}}$ signal and therefore the repetition rate period (42.5Ω sec) is the same as the $\overline{\text{SHIFT}}$ signal. The train of DATA STROBE pulses appears at output pin A305-38 of the FSK receiver and is applied to pin A12-39 of the message/bit counter in the selected message control circuits.

INPUT AT TRU OUTPUT CONNECTOR J3



FSK FORMAT

1. SYNC CHARACTER ALWAYS APPEARS AT START OF MESSAGE, BEFORE TRAIN OF DATA BITS.
2. SYNC CHARACTER CHANGES ONCE EVERY TWO DATA BIT PERIODS (APPROX 85 μSEC)
3. DATA BIT ZERO CHANGES ONCE EVERY DATA BIT PERIOD (APPROX 42.5 MS)
4. DATA BIT ONE CHANGES ONCE EVERY 1/2 DATA BIT PERIOD (APPROX 21.3 MS)

A61036-9

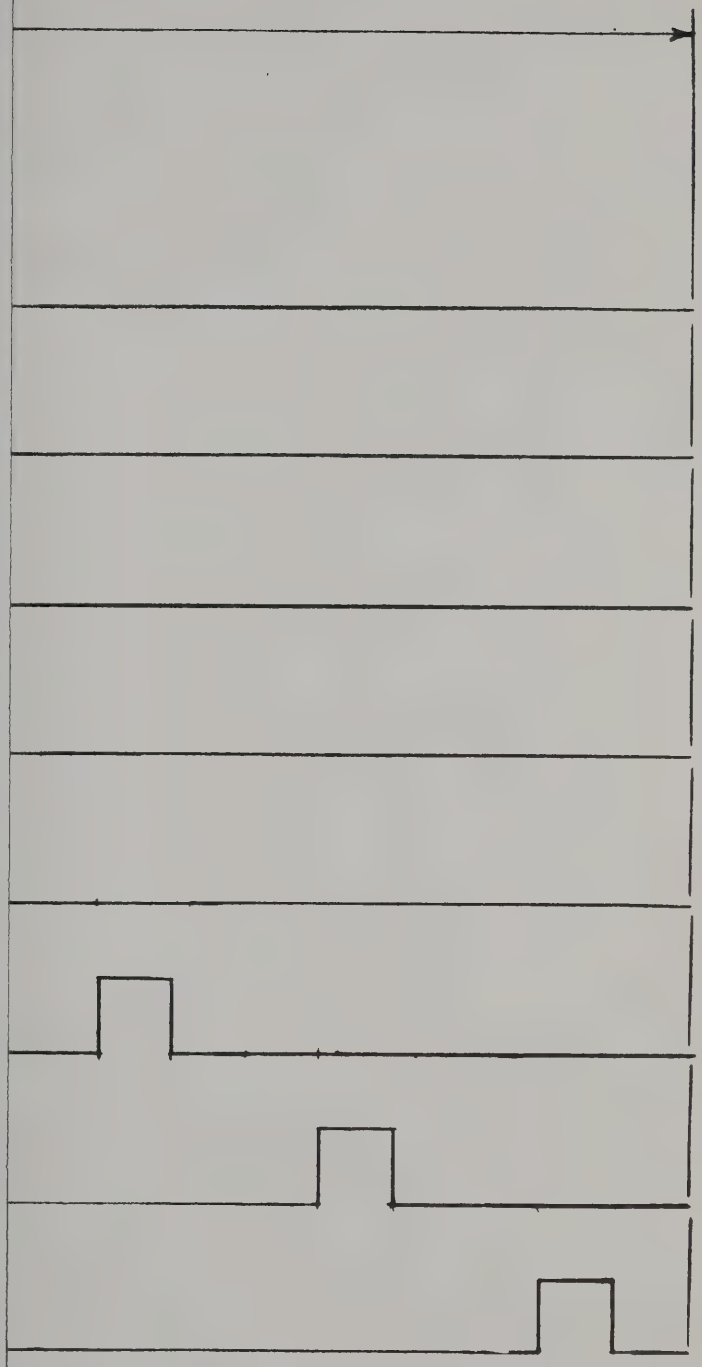
FIGURE 4-4. INPUT TEST MESSAGE, FSK CODED FORMAT

4-19. The FSK receiver is clocked by a 5.18 MHz clock from the FSK clock circuits. (The 5.18 MHz clock is equivalent to 1/64 nautical mile (nm) or about 0.2 μsec clock.) Two clocks are then internally generated by the FSK receiver A305. One clock, known as the D or 10/64 nm clock, appears at pin A305-25. The D clock is jumpered back to pins A305-40 and A305-26 for use as the DATA clock and COUNT clock, respectively. The other internally generated clock is known as the B clock and appears at pin A305-23. The B clock is jumpered back to pin A305-21 as the DATA STROKE clock.

4-20. After the end of sync character period in the input test message, a $\overline{\text{SYNC}}$ signal appears at output pin A305-34 of the FSK receiver and is applied to pin A307-25 of the count reset control gates and to pin A304-17 of the message/bit counter in the selected message control circuit. A SHIFT signal is generated once every data bit period, or approximately 42.5 μsec except when a sync signal is present. The train of $\overline{\text{SHIFT}}$ pulses appears at output pin A305-14 of the FSK receiver and is applied to pin A306-21 of the shift clock gates. In every data bit period, a DATA STROBE signal is generated immediately after the $\overline{\text{SHIFT}}$ signal and therefore the repetition rate period (42.5Ω sec) is the same as the $\overline{\text{SHIFT}}$ signal. The train of DATA STROBE pulses appears at output pin A305-38 of the FSK receiver and is applied to pin A12-39 of the message/bit counter in the selected message control circuits.

4-21. Shift Clock Gates. Inputs to the shift clock gates are the $\overline{\text{SHIFT}}$ signal from the FSK receiver and the $\overline{\text{EOM}}$ signal from the selected message control circuits. Outputs of the shift clock gates are the bit, data, and shift clocks applied to the selected message control circuits and FSK data register circuits.

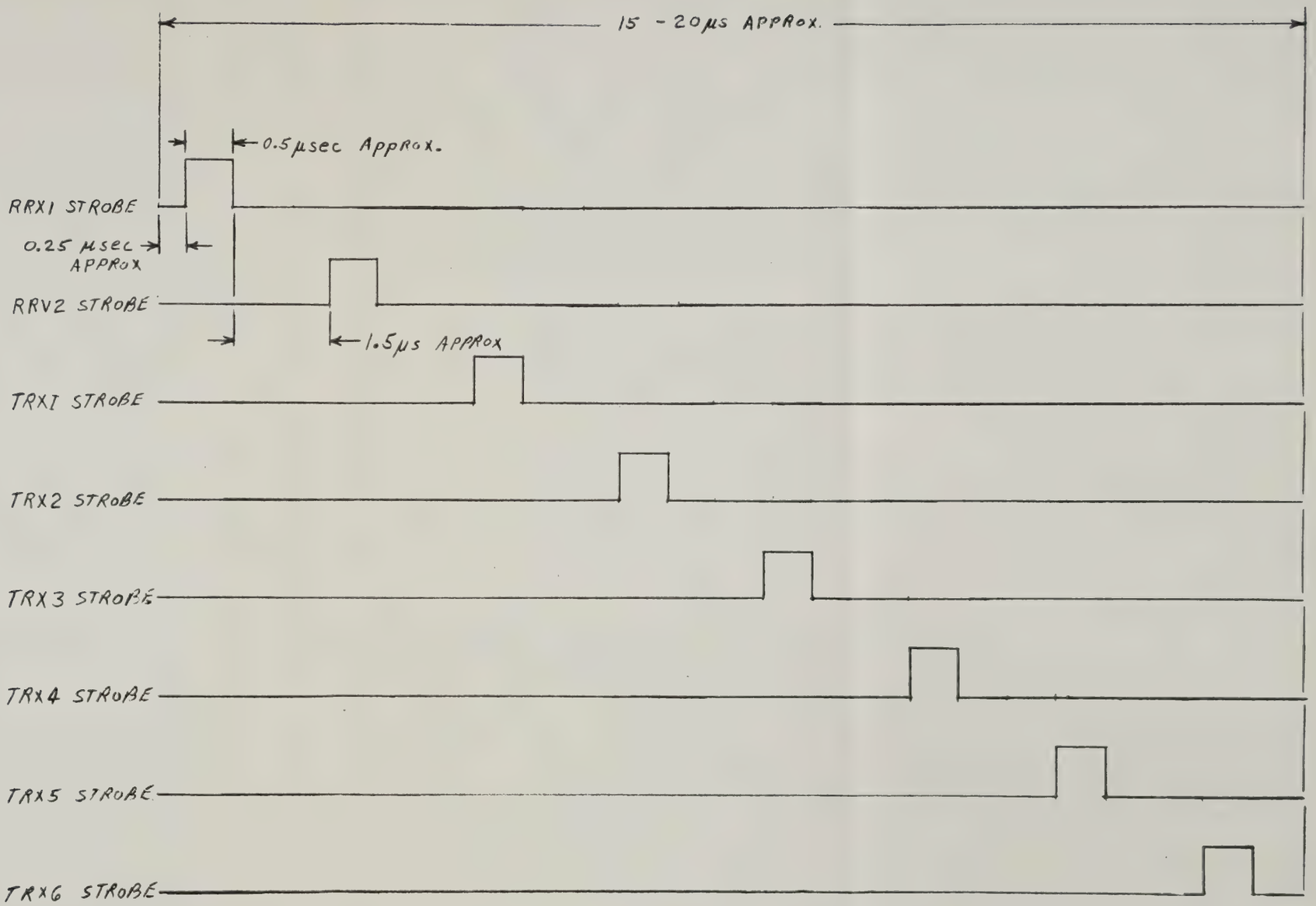
4-22. The $\overline{\text{SHIFT}}$ signal from FSK at pin A305-14 is inverted by inverter A306-U2B and the resultant output SHIFT clock signal appears at pin A306-23 for application to the selected message control circuits and as one input to bit clock gate A306-U2C. The other input to the gate is the $\overline{\text{EOM}}$ signal from the selected message control circuits. Until the end of the data message period, the $\overline{\text{EOM}}$ signal is high. Thus, with the train of positive-going pulses of the SHIFT signal from inverter A306-U2B as input, gate A306-U2C provides a train of negative-going pulses as the bit clock output at pin A306-24. The bit clock output is applied to the selected message control circuits to clock the bit counting function of those circuits. The bit clock is also inverted by inverter A310-U8A and the resultant data shift clock, consisting of a train of positive-going pulses, appears at pin A310-7 for application to the FSK data register circuits. The data shift clock is used to shift the DATA signal from the FSK decoding circuits serially into registers for parallel display on the test set control panel.



A61036-10

4-21. Shift Clock Gates. Inputs to the shift clock gates are the $\overline{\text{SHIFT}}$ signal from the FSK receiver and the $\overline{\text{EOM}}$ signal from the selected message control circuits. Outputs of the shift clock gates are the bit, data, and shift clocks applied to the selected message control circuits and FSK data register circuits.

4-22. The $\overline{\text{SHIFT}}$ signal from FSK at pin A305-14 is inverted by inverter A306-U2B and the resultant output SHIFT clock signal appears at pin A306-23 for application to the selected message control circuits and as one input to bit clock gate A306-U2C. The other input to the gate is the $\overline{\text{EOM}}$ signal from the selected message control circuits. Until the end of the data message period, the $\overline{\text{EOM}}$ signal is high. Thus, with the train of positive-going pulses of the SHIFT signal from inverter A306-U2B as input, gate A306-U2C provides a train of negative-going pulses as the bit clock output at pin A306-24. The bit clock output is applied to the selected message control circuits to clock the bit counting function of those circuits. The bit clock is also inverted by inverter A310-U8A and the resultant data shift clock, consisting of a train of positive-going pulses, appears at pin A310-7 for application to the FSK data register circuits. The data shift clock is used to shift the DATA signal from the FSK decoding circuits serially into registers for parallel display on the test set control panel.



A61036-10

FIGURE 4-5. TIMING SEQUENCE OF TARGET AND REPLY TRANSFER STROBE INPUTS

4-23. SELECTED MESSAGE CONTROL CIRCUITS BLOCK DIAGRAM DISCUSSION. The selected message control circuits consist of antenna position control gates, count reset control gates, and a message/bit counter (refer to figure 4-2). The basic functioning of the selected message control circuits is to count the FSK-coded input test messages (starting from number one) as received at the test set, until the count designated by the proper setting of applicable control-panel TARGET SELECTION switches is reached. After this selected test message has been reached and is to be converted by the FSK decoding circuits, the selected message control circuits then function to count the number of data bits being serially inserted into the FSK decoding circuits. During the message period, the selected message control circuits provide signals for timing control of the message parity checker. At the end of the message period, the bit counting function of the selected message control circuits stops. The selected message control circuits do not start message counting operation again until the message output of the Video Signal Processor is cycled back to message number one, that is, until just before the beacon radar antenna of the Video Signal Processor completes a full scan.

4-24. Message Selection and Counting Function. For the selection of any specific message, applicable TARGET SELECTION switches on the control panel are set to the up position and the TARGET SELECTION ALL switch is set to the down position. The resultant $\overline{\text{ALL}}$ signal is an enabling high-level

input to the antenna position control gates. When the nearly full antenna scan, as prepresented by the input AZ3 to AZ11 bits, is reached, the circuit enable signal output of the antenna position control gates goes high. This high-level count enable signal then serves to condition the message/bit counter to count input test messages once the number of the selected message is determined by the settings of the applicable TARGET SELECTION switches.

4-25. As determined by the settings of the applicable TARGET SELECTION switches, the logic status of the seven target selection control signals establishes a binary count equal to the 7-bit full count (127) less the number of the selected message. This binary count together with the high-level count enable signal from the antenna position control gates cause the message/bit counter to be preset to this input binary count. For example, assume that message number two is to be selected for display by the control-panel OUTPUT indicator lamps. On the control panel, TARGET SELECTION 2 switch is set to the up position, with all other TARGET SELECTION switches set to the down position. These switch settings provide a low level on the target selection control line associated with the TARGET SELECTION 2 switch and a high level on each of the other six target selection control lines. The logic status of these seven lines forms a binary count of 125, which is full count, 127, less two, the number of the message to be selected. This binary count input presets the message/bit counter to a count of 125.

4-26. The $\overline{\text{TRU START}}$ input signal to the message/bit counter from the Video Signal Processor is a narrow negative-going pulse that appears in sync with the reception of the FSK-coded message, that is, with the reception of the $\overline{\text{TRU OUTPUT}}$ input to the test set. Thus, the $\overline{\text{TRU START}}$ input pulse appears every time a message is received. A count of the number of $\overline{\text{TRU START}}$ pulses appearing at the test set input is therefore a count of the number of FSK-coded messages received. Again, assume that message number two is to be selected. The message/bit counter is preset to a count of 125. The appearance of two $\overline{\text{TRU START}}$ input pulses clock the message/bit counter to the full count of 127. Thus, the second message or second $\overline{\text{TRU START}}$ pulse completes the count.

4-27. At this time, the message/bit counter provides a low-level selected message count signal to the count reset control gates. After the receipt of the negative-going leading edge of the $\overline{\text{SYNC}}$ pulse from the FSK receiver, the count reset control gates generate a low-level $\overline{\text{RESET}}$ signal which is fed back to reset the message/bit counter. (The $\overline{\text{SYNC}}$ pulse represents the reception and decoding of the input test message by the FSK decoding circuits.) The $\overline{\text{RESET}}$ signal remains low level until the positive-going trailing edge of the $\overline{\text{SYNC}}$ pulse is received. Once the $\overline{\text{RESET}}$ signal goes positive, the message/bit counter can be clocked again for the start of a counting operation. Counting is now under control of the bit clock from the shift clock gates on the FSK decoding circuits. Counting starts from a zero count, that is,

the message/bit counter does not preset to a count because the count enable signal input from the antenna increment control gates, due to accompanying changes in the azimuth position input bits to AZ3 to AZ11, becomes an inhibiting low level. Since the bit clock represents data bit periods, the message/bit counter now functions to count, starting from zero, the number of serial data bits being received by the FSK decoding circuits at the $\overline{\text{TRU OUTPUT}}$ input connector of the test set.

4-28. Bit Counting Function. The message/bit counter keeps counting the number of serial data bits in the input FSK-coded test message until the full bit count of 88 is reached. At this time, high-level full bit count and high-level EOM signals are applied to the count reset control gates. At the trailing edge of the 88th shift clock input from the shift clock gates of the FSK decoding circuits, the count reset control gates then generate a low-level $\overline{\text{RESET}}$ signal, which is fed back to reset the message/bit counter. Under these conditions, the $\overline{\text{RESET}}$ signal remains low level until the negative-going leading edge of the 89th shift clock is received. Once the $\overline{\text{RESET}}$ signal goes positive, the message/bit counter can be clocked again for the start of selected message counting operation, once the beacon radar antenna reaches near full scan.

4-29. Parity Checker Control Function. During the message period, the message/bit counter of the selected message control circuits counts groups of eight data bits and provides, after every eighth data bit, two signals (PARITY STROBE and $\overline{\text{PARITY STROBE}}$), which are used for the parity

checking function of the message parity checker. At the end of the message, the message/bit counter provides a high-level PARITY CONTROL signal that permits the message parity checker to complete the check of parity in the message. At the start of the next message, the PARITY CONTROL signal goes low to inhibit the functioning of the message parity checker until the end of the message.

4-30. Reset Operations. The resetting of the message/bit counter is controlled by the count reset control gates and occurs at three different times: at start of message counting, after the end of message counting, and at end of message bit counting. Inputs to the count reset control gates are:

a. The $\overline{\text{ALL}}$ signal determined by the setting of the TARGET SELECTION ALL switch on the control panel.

b. The two start reset control signals from the antenna position control gates.

c. The $\overline{\text{TRU START}}$ input signal from the Video Signal Processor.

d. The full bit count (88), the selected message count and the EOM signals from the message/bit counter.

e. The $\overline{\text{SYNC}}$ and shift clock signals from the FSK decoding circuits.

Outputs are the $\overline{\text{RESET}}$ and $\overline{\text{GO-SYNC}}'$ signals.

4-31. After power turn-on and at the start of message counting, which occurs just after the beacon radar antenna has reached near full scan, (358.6°), the two start reset signals are each high level. With these high-level inputs,

the count reset control gates produce a low-level $\overline{\text{RESET}}$ signal to reset the message/bit counter at the start of message counting. The $\overline{\text{RESET}}$ signal remains low level until the beacon radar antenna reaches 359.3°, at which time one of the two start reset signal goes to low level. Once the $\overline{\text{RESET}}$ signal output of the count reset control gates goes high level, the message/bit counter is no longer held reset and can then start functioning as a message counter. If all test messages are to be displayed, the control panel TARGET SELECTION ALL switch is set to the up position. The resultant $\overline{\text{ALL}}$ signal input to the count reset control gates is a high level, inhibiting the gates. As a result, the count reset control gates provide a steady high-level $\overline{\text{RESET}}$ input to the message/bit counter as long as this all test message condition is maintained. Since the message/bit counter is never reset under the all test message condition it is not used for message (or data bit) counting.

4-32. When the selected input FSK-coded test input message has been reached and received by the test set, the count reset control gates receive a low-level selected message count signal from the message/bit counter, indicating the end of the message counting function performed by the counter. At this same time (the start of selected message period), the $\overline{\text{TRU START}}$ input to the count reset control gates is a low level. Thus, the low-level selected message count, $\overline{\text{TRU START}}$, and $\overline{\text{ALL}}$ inputs so condition the count reset control gates that when the negative-going leading edge of the

$\overline{\text{SYNC}}$ signal is received from the FSK decoding circuits, the count reset control gates can then provide the required low-level $\overline{\text{RESET}}$ signal. The $\overline{\text{RESET}}$ signal clears the message/bit counter for the message bit counting function next to be performed by the message/bit counter. This functioning starts once the $\overline{\text{RESET}}$ signal goes positive, which occurs at the positive-going trailing edge of the $\overline{\text{SYNC}}$ input to the count reset control gates (refer to paragraph 4-27). Thus, the $\overline{\text{RESET}}$ pulse output at the end of message counting is a narrow low-level pulse, whose width is the same as the pulse width of the input $\overline{\text{SYNC}}$ pulse.

4-33. Under the all message condition, the $\overline{\text{ALL}}$ input from the control panel to the count reset control gates is high-level. This high-level signal inhibits the gates to provide a high-level $\overline{\text{RESET}}$ signal, preventing the message/bit counter from being cleared or used as a counter (refer to paragraph 4-31). The count reset control gates also provide, at the same time as the $\overline{\text{RESET}}$ signal, low-level $\overline{\text{GO SYNC}}$ signals that are used to reset the bit parity status checker in the message parity checker circuits and to condition the message/bit counter for the generation of control signals at the end of message.

4-34. At the end of the bit counting operation of the message/bit counter, high-level full bit count and EOM signals are applied to the count reset control gates from the message/bit counter. Under control of the shift clock pulses from the FSK decoding circuits, the count reset control gates provide

the required low-level $\overline{\text{RESET}}$ output used to clear the message/bit counter for message counting once the beacon radar antenna reaches near full scan and the cycle of test messages comes back to test message no. 1.

4-35. SELECTED MESSAGE CONTROL CIRCUIT ANALYSIS. The following paragraphs discuss the circuit analysis of the functions of the selected message control circuits. This discussion is supported by test set and circuit card schematics in T.O. 33D7-24-13-3.

4-36. Message Selection and Counting Function. For the selection of any specific test message, applicable TARGET SELECTION switches on the control panel are set to the up position and the TARGET SELECTION ALL switch is set to the down position. The resultant $\overline{\text{ALL}}$ signal from control panel A1S12 switch is a high-level input at pin A311-12 to A311-U1A in the antenna increment count control circuits. When the nearly full antenna scan (359.3°) as represented by all high-levels on the AZ3 to AZ11 position bits, is reached, the other inputs to A311-U1A at pins A311-8 and 10 of all become high through inversion by A306-U4C and U4D, and after detection by target count detector A311-U4. The resultant output at pin A311-14 is low level, and after inversion by A306-U4A, a high-level count enable signal is applied to the message/bit counter at pins A306-26 and 1.

4-37. Assume that message number two is to be selected. On the control panel A1, TARGET SELECTION 2 switch A1S6 is set to the up position, with all other TARGET SELECTION switches set to the down position. These switch settings provide a low level on the target selection control line input to A306-3B at pin A306-29 and a high level on each of the other six target selection control line inputs to gates A306-U3A, U3C, U3D, U1A, U1B, and U12. Since the high-level count enable signal from pin A306-37 of gate A306-U4A is an input to all these gates, the low-level target selection control line 2 inhibits gate A306-U3B, with all other gates enabled by the high-level target selection control lines. As a result, all flip flops comprising a seven-stage binary counter are set except flip flop A303-U1B, which is kept from setting by the high-level output from gate A306-U3B. Thus, the seven-stage binary counter is preset to the binary count of 125, which is the full count of the counter less two, the number of the test message to be selected.

4-38. The $\overline{\text{TRU START}}$ input at connector A1J6 of the test set is applied as input to gate A306-U2D at pin A306-14. After inversion by A306-U2D and A310-U2A, the $\overline{\text{TRU START}}$ input pulses from the Video Signal Processor clocks the seven-stage binary counter at every negative-going edge of the pulses. With the binary counter preset to 125, only two clock pulses applied to the counter at pin A303-1 from pin A310-22 of inverter A310-U2A are required to complete the full count (refer to T.O. 33D7-24-13-3). Since the

clocking $\overline{\text{TRU START}}$ input pulse appears every time a message is reached, full count is obtained when message number two (or the second $\overline{\text{TRU START}}$ pulse) is received by the test set.

4-39. When the second test message is received, the seven-stage counter A303-U1A, U1B, U2A, U2B, U3A, and A304-U3A and U3B is at full count of 127 and the high-level binary outputs of the counter are applied as inputs to full count detector A312-U3 of the count reset control circuits. The seven-stage binary counter is then reset by a low-level $\overline{\text{RESET}}$ signal from inverter A310-U6A at pin A310-34. When the $\overline{\text{RESET}}$ signal goes positive (at the start of bit counting), the seven-stage binary counter can be clocked again for the start of a counting operation. (Refer to paragraph 4-46 for the reset operation.) When the $\overline{\text{RESET}}$ signal is removed, the seven-stage binary counter holds at a zero count since all seven outputs of the seven target selection control gates are now at an inhibiting high level. These high-level outputs result from the fact that the input antenna position bits AZ3 thru AZ11 are no longer all at high level, thereby inhibiting position gate A311-U1A. The high-level signal output at pin A311-14 is inverted by A306-4A to provide a low-level count enable signal at pin A306-37. The low-level count enable signal thus serves to inhibit the seven target selection control gates, preventing the seven-stage binary counter from being presetted.

4-40. Bit Counting Function. Counting is now under control of the bit clock from the shift clock gates in the FSK decoding circuits. The bit clock pulses are applied to clocking gate A306-U2D at pin A306-16. The clock output of gate A306-U2D at pin A306-18 is inverted by inverter A310-U and the output at pin A310-22 is applied to clock the seven-stage binary counter at the negative-going edge of each clock pulse. Since the bit clock represents data bit period, the binary counter starts counting, from zero, the number of serial data bits being received by the FSK decoding circuits at the $\overline{\text{TRU OUTPUT}}$ input connector of the test set.

4-41. The seven-stage binary counter keeps counting the number of serial data bits until the full bit count of 88 is reached. At this time, the binary outputs of the counter adding to 88, that is the BC8, BC16, and BC32 outputs, are applied as high-level inputs to bit count detector A311-U at pins A311-16, A311-18, and A311-20, respectively. The low-level output of the detector at pin A311-24 is inverted by inverter A307-U3C with the resultant high-level output, known as the 88 signal, appearing at pin A307-30. The 88 signal is applied to pin A304-24 of end of message generator flip flop A304-U2B and is used to condition the flip flop for the generation of a high-level EOM signal at the negative-going trailing edge of the PARITY STROBE signal (at the 88th bit clock pulse). The PARITY STROBE signal is derived from parity sample detector A312-U4B through inverter A310-U8A and is applied to pin A304-19

to clock the end of message generator flip flop A304-U2B. (Refer to paragraph 4-43 for the parity checker control function operation.)

4-42. Both the high-level 88 signal from bit count detector A311-U and the high-level EOM from end of message flip flop A304-U2B are applied as inputs to end of message reset gate A312-U at pins A312-15 and 17, respectively. The seven-stage binary is then reset by a low-level $\overline{\text{RESET}}$ signal from inverter A310-U6A at pin A310-34. When the $\overline{\text{RESET}}$ signal goes positive (at the 89th shift clock), the seven-stage binary counter can then be clocked again for the start of a counting operation. (Refer to paragraph 4-46 for the reset operation.)

4-43. Parity Checker Control Function. During the test message period, the $\overline{\text{BC1}}$, $\overline{\text{BC2}}$, and $\overline{\text{BC4}}$ binary outputs of the seven-stage binary counter are applied to pins A312-40, 38, and 36, respectively as inputs to parity sample detector A312-U4B. These three inputs become high levels at the leading edge of every eighth bit clock. The other two inputs to parity sample detector A312-U4B are the DATA STROBE signal, applied at pin A312-39 from the FSK receiver, and the $\overline{\text{EOM}}$ signal applied at pin A312-34 from the end of message flip flop A304-U2B. The DATA STROBE signal is a train of high-level pulses, with a pulse appearing at the trailing edge of each bit clock, and the $\overline{\text{EOM}}$ signal is high level until the trailing edge of

the 88th bit clock. Thus, at every eighth bit clock including the 88th, all inputs to parity sample detector A312-U4B are high level. The output of detector A312-U4B at pin A312-31 is the negative-going $\overline{\text{PARITY STROBE}}$ signal and is applied to inverter A310-U8A at pin A310-2 to produce the positive-going PARITY STROBE signal (refer to T.O. 33D7-24-13-3). At the leading edge of each 8th bit clock, the DATA STROBE signal goes negative, thereby inhibiting parity sample detector A312-U4B. The $\overline{\text{PARITY STROBE}}$ signal at pin A312-31 then goes positive, and the complement PARITY STROBE signal at pin A310-2 goes negative. Thus, the PARITY STROBE signal is a narrow low-level pulse and the complement PARITY STROBE signal is a narrow high-level pulse appearing at every 8th bit clock.

4-44. The low-level $\overline{\text{PARITY STROBE}}$ signal is applied at pin A307-15 to be parity error flip flop A307-U2A, with every 8th pulse setting the flip flop. The PARITY STROBE signal is applied to each flip flop in the bit parity status checker of the message parity checker circuits, with the leading edge of each PARITY STROBE pulse clocking each flip flop. The PARITY STROBE signal is also applied to end of message flip flop A304-U2B at pin A304-19, clocking the flip flop at the leading edge of the signal. No change in the state of flip flop A304-U2B occurs until the 11th clock, that is, at the 88th bit. The $\overline{\text{EOM}}$ output of flip flop A304-U2B at pin A304-25 is

thus high-level for the length of the data message period and goes to low level at the leading edge of the PARITY STROBE clock input. Similarly, the complement EOM output at pin A304-22 goes positive at the leading edge of the PARITY STROBE clock input. Since the $\overline{\text{EOM}}$ signal is applied to parity sample detector A312-U4B, the detector is inhibited after the 88th bit clock and is not enabled until the start of a new test message (when selected and accepted) permits the $\overline{\text{EOM}}$ signal to go to high level. The low-level $\overline{\text{EOM}}$ signal is also applied to the FSK decoding circuits at pin A306-22 to inhibit the bit clock gates in these circuits. (Refer to paragraph 4-21 for a detailed circuit analysis of the shift clock gates.)

4-45. The complement EOM signal output signal at pin A304-22 is applied to the parity control flip flop A-304-2A at pin A304-18. At the 89th shift clock, that is, after end of message, this flip flop provides a high-level PARITY CONTROL output at pin A304-26 to enable the control gate A307-U1C of the message parity checker circuits (refer to paragraph 4-57). The EOM signal is also applied to the end of message reset gate A312-U2B at pin A312-17 to permit the resetting of the seven-stage binary counter (refer to paragraph 4-46).

4-46. Reset Operations. As noted in paragraph 4-30, the resetting of the seven-stage counter in the message/bit counter circuits occurs at three different times: at start of message counting, after the end of message counting, and at end of message bit counting. When the beacon radar antenna

reaches 358.6° (just prior to the start of message counting), the AZ4 to AZ11 input azimuth position bits are all high level and AZ3 inputs bits are low level. The low-level AZ3 input is inverted by inverter A306-U1D, with the high-level output applied as a start reset signal (AZ3) to message start reset gate A311-U1B at pin A311-3. The high-level AZ4 through AZ11 inputs are applied to target count detector A311-U4B, whose low level output is inverted by inverter A306-4D to produce a high-level start reset signal (AZ4 - AZ11). This high-level reset signal is applied to message start reset gate A311-U1B at pin A311-1.

4-47. Prior to the start of message counting, the $\overline{GO}$ signal from reset flip flop gate A312-U1A at pin A312-14 is a high level and is applied to the message start reset gate A311-U1B at pin A311-5. The remaining input of the reset gate A311-U1B is the high-level $\overline{ALL}$ signal from TARGET SELECTION ALL switch A1S12, set to the down position. With all these inputs to reset gate A311-U1B at high level, the gate output is a low level and is applied as an enabling low-level signal to the counter reset gate A311-U2B at pin A311-13. The output of counter reset gate A311-U2B is a high level to be inverted by inverter A310-U6A to provide the required low-level $\overline{RESET}$ signal at pin A310-34. The $\overline{RESET}$ signal remains low level until the beacon radar antenna scan increments 0.7 degrees, causing the AZ3 input to the test set to become a high level. The $\overline{AZ3}$ input to the start of message gate A311-U1B on pin A311-3 is now an inhibiting low level, causing the gate output to become a high-level signal. This high-level signal inhibits counter reset gate A311-U2B, whose output

after inversion by inverter A310-U becomes a high level $\overline{\text{RESET}}$ signal. Thus, the seven-stage binary counter is held reset by a low-level $\overline{\text{RESET}}$ signal for the time of a 0.7-degree increment in the beacon radar antenna scan.

4-48. If all the test message are to be displayed, the control panel TARGET SELECTION ALL switch A1S12 is set to the up position . The resultant low-level $\overline{\text{ALL}}$ signal inhibits the message start gate A311-U1B, causing the output of the gate to be high level, which in turn, inhibits counter reset gate A311-U2B. Thus, the $\overline{\text{RESET}}$ signal output of inverter A310-U is now a steady high level, preventing the seven-stage binary counter from being reset under the all test message condition.

4-49. When message counting by the seven-stage binary counter is completed, the binary outputs of the counter are all high-level and are applied as inputs to message count gate A312-U3A. The resultant low-level output is applied to control gate A307-U2C which provides a high-level input to the reset control gate A312-U1B at pin A312-1. When the low-level $\overline{\text{SYNC}}$ pulse from the FSK decoding circuits is received at sync gate A307-U3A on pin A307-26, the output of the gate becomes the high-level SYNC' signal that is applied as an enabling signal to the reset control gate A312-U1B at pin A312-3. The resultant low-level output is then applied to the reset flip flop A307-U2B.

4-50. Prior to the receipt of the SYNC' signal, the reset flip flop was reset by the applicable low-level $\overline{\text{TRU START}}$ input pulse applied at pin A307-8.

The low-level input to the reset control flip flop gate A307-U2C now sets the flip flop, providing a high-level GO signal at pin A307-22. The complement $\overline{GO}$ signal becomes low level. Since the reset control flip flop is reset only when the low-level end of message (EOM) signal from flip-flop A304-U2A is applied at pin A307-10, the GO signal is kept at high level throughout the complete message data period. (Refer to T.O. 33D7-24-13-3.) The high-level GO signal is applied as one input to the go gate A307-U1A at pin A307-1. Since the other input to this gate is the high-level SYNC' input on pin A307-3, the gate is enabled, providing a low-level $\overline{GO\ SYNC'}$ signal output on pin A307-5. This low-level $\overline{GO\ SYNC'}$ signal is applied as an enabling signal to counter reset gate A311-U2B, whose high level output becomes after inversion by inverter A310-U6A the required low-level $\overline{RESET}$ signal. The $\overline{RESET}$ signal remains low level until the SYNC' signal input to the go gate A307-U1A goes negative, which occurs, of course, when the $\overline{SYNC}$ signal from the FSK decoding circuit goes positive. The negative-going SYNC' signal inhibits the go gate A307-U/A, thereby providing a high-level input to inhibit counter reset gate A311-U2B. Thus, the $\overline{RESET}$ pulse output at the end of message counting is a narrow low-level pulse, whose width is the same as the pulse width of the input $\overline{SYNC}$ pulse.

4-51. The GO signal output of the reset flip flop A307-U2B is also applied to another go gate A310-U on pin A310-13. Again, the receipt of a high level SYNC' signal from sync gate A307-U3A on pin A310-15 enables the go

gate A310-U4A. The output of this gate is another low level $\overline{\text{GO SYNC}}'$ signal. Thus there are now two $\overline{\text{GO SYNC}}'$ signals derived from two different go gates. The $\overline{\text{GO SYNC}}'$ signal from go gate A307-U2B is applied to the end of message flip flop A304-U2B on pin A304-20 to set this flip flop. The $\overline{\text{EOM}}$ output at pin A304-25 is thus high level and remains high level until the flip flop is conditioned by the high-level 88 input from inverter A307-U3C at the end of message and the flip-flop is clocked by the leading edge of the PARITY STROBE clock. The other $\overline{\text{GO SYNC}}'$ signal from go gate A310-U4A is applied as the reset signal for all the flip-flops in the bit parity status checker. This $\overline{\text{GO SYNC}}'$ signal goes positive to remove the reset from the parity status checker flip flops when the SYNC' signal input to go gate A310-U4A goes negative. The SYNC' signal goes negative when the $\overline{\text{SYNC}}$ signal input to sync gate A307-U3A goes positive, that is, at the trailing edge of the $\overline{\text{SYNC}}$ pulse. Thus, the parity status checker flip flops are held reset for the width of the $\overline{\text{SYNC}}$ pulse from the FSK decoding circuits prior to the start of data bit processing.

4-52. At the end of the bit counting operation of the seven-stage binary counter in the message/bit counter circuits, a high-level 88 signal is available from bit count detector A311-U2A (after inversion by inverter A307-3C) at pin A307-30. (Refer to paragraph 4-41.) This high-level 88 signal is applied as one input to the end of message detector A312-U2B at pin A312-15. At the end of the data message, a high-level EOM signal is available from end of message flip flop A304-U2B at pin A304-22. (Refer to paragraph 4-45). This high-level EOM signal at end of message is

applied as another input to the end of message detector A312-U2B at pin A312-17. Another input to the end of message detector A312-U2B at pin A312-13 is the GO signal from reset flip flop A307-U2B. At the end of the message period, the GO signal is high level. (Refer to paragraph 4-50.) The remaining input to the end of message detector A312-U2B at pin A312-11 is the shift clock pulses from the FSK decoding circuits. At the positive going trailing edge of the 88th shift clock pulse, all inputs to the end of message detector A312-U2B are high level.

4-53. The resultant output of the end of messager detector A312-U2B is a low level, which is applied to counter reset gate A311-U2B on pin A311-15. The high-level output of this gate on pin A311-19 is marked by inverter A310-U6A to produce the required low-level $\overline{\text{RESET}}$ signal used to reset the seven-stage binary counter. The $\overline{\text{RESET}}$ signal remains low level until the negative-going leading edge of the next (89th) shift clock input is received to inhibit the end of message detector A312-U2B and in turn, to inhibit the counter reset gate A311-U2B (through inverter A310-U) from providing a low-level $\overline{\text{RESET}}$ signal.

4-54. MESSAGE DATA REGISTER CIRCUITS.

4-55. Block Diagram Discussion. The 88 bits of data from the FSK receiver of the FSK decoding circuits are applied serially to the 8-bit serial-in parallel-out shift registers and are shifted in by means of the data clock from the shift clock gates (paragraph 4-21). There are 11 shift registers, with each register handling eight data bits which appear on eight

parallel outputs. Each of the 88-bit parallel data outputs is applied to an inverter, whose output drives a light emitting diode in the OUTPUT section of the control panel. When all 88 bits of data are serially clocked in to the shift registers, the data bits including parity bits are then completely displayed by the OUTPUT display lamps. In addition, each group or bite of 8 data bits, as serially clocked in, is applied to the message parity checker for check of parity in the message.

4-56. Circuit Diagram Analysis. The 11 shift registers are contained on three DDL type printed cards A308, A208, and A108. All shift registers are serially connected on each card and between cards, with the 88-bit data from the FSK receiver applied to the first shift register A308-U1 at pin A308-5. The data clocks are applied to each card at pins A108-2, A208-2, and A308-2. The data on the parallel outputs of the shift registers are applied to inverters contained on printed circuit cards A105, A106, A107, A206, A207, and A310. The outputs of the inverters drive light emitting diodes on control-panel indicator assemblies 1A1A1, 1A1A2, and 1A1A3 to form the OUTPUT display. Each group of eight data bits as clocked through the first shift register A308-U1 on DDL printed circuit card A308 is applied to those flip flops on printed circuit cards A309 and A304, which form the bit parity status checker.

4-57. MESSAGE PARITY CHECKER.

4-58. Block Diagram Discussion. At the start of the test message, the bit parity status checker is reset by the $\overline{\text{GO SYNC}}$ signal from the count reset control gates in the selected message control circuits.

The 88 bits of the data message on the parallel outputs of the shift registers in the FSK data register circuits are examined, in group of eight bits, for the number of logic 1's contained in the message. Parity for this system is odd parity, that is, the number of logic 1's in the message must be an odd number. If the parity count is correct, all high level parity comparison signals (P1 thru P8) are applied from the bit parity status checker to the correct parity detector after the last eight bits of the data message has been examined. The resultant output is the low-level parity status signal applied to a control gate which is conditioned by a high-level PARITY CONTROL signal from the selected message circuits. Under this condition, the output of the control gate is a high-level parity status signal that is applied to the reset input of the parity error flip flop circuit. The flip flop had been set by the negative-going leading edge of the last (11th) $\overline{\text{PARITY STROBE}}$ signal from the message/bit counter. However, the high-level parity status signal does not reset the flip flop circuit, and consequently the output of the flip flop circuit is a high-level parity error signal that does not light the PARITY ERROR lamp in the OUTPUT display section of the test set control panel.

4-59. If the parity count is not correct, that is, the count is even, the parity comparison signal inputs to the correct parity detector from the bit parity status checker are not all high levels. Consequently, the parity status output of the detector is now a high-level signal applied to the control gate conditioned by the high-level PARITY CONTROL signal. Under this condition, the output of the control gate is a low-level parity status signal.

This low-level parity status signal resets the previously set parity error flip flop circuit. The output of the circuit is now a low-level parity error signal that causes the PARITY ERROR lamp to light as indication of a detection of an error in the odd parity count.

4-60. Detailed Circuit Analysis. The bit parity status checker consists of eight flip flops, A309-U1A, U1B, U2A, U2B, U3A, and U3B and A304-U1A, U1B. Just after the start of the FSK-coded data message conversion, each flip flop is reset by the low-level $\overline{\text{GO SYNC}}$ signal from the count reset control gates (refer to paragraph 4-51). Each flip flop is clocked at the trailing edge of each PARITY STROBE pulse from the message/bit counter in the selected message circuit. A PARITY STROBE pulse appears at every eighth shift clock, that is, at every eighth data bit (refer to paragraphs 4-43 and 4-44). Each data bit of each group of eight bits is applied to both inputs of a corresponding flip flop in the bit parity status checker. Depending upon the logic status of these data bits, the flip flops, when clocked by each of the 11 PARITY STROBE signals during the test data message period, changes or does not change state, starting from the logic 0 existing at reset. If the data bit input to the flip flop is a logic 1, the corresponding flip flop changes state; if the data bit is a logic 0, the corresponding flip flop does not change state.

4-61. If any flip flop changes state an odd number of times during the 11 clockings, then the number of logic 1 data bits examined by the flip flop is a correct odd number; if the flip flop changes state an even number of times, then the number of logic 1 data bits examined is an incorrect even number. In effect, each flip flop of the bit parity status checker circuits examines a column of 11 data bits and if each column has the correct odd number of logic 1's, then the final state of each flip flop, at the 11th PARITY STROBE clocking, is a high level. Thus, if the data message of 88 bits contains the correct odd number of logic 1's, then the parity comparison P1 through P8 inputs to the correct parity detector A311-U3A are all high levels.

4-62. The resultant parity status output of the correct parity detector A311-U3A at pin A311-29 is a low level to be applied as one input to the control gate A307-U1C at pin A307-10. The other input to this gate at pin A307-8 is the PARITY CONTROL signal from pin A304-26 of the parity control flip flop A304-2A in the message/bit counter. Until the 88th shift clock, the PARITY CONTROL signal is a low level, but at the first shift clock (89th) after the end of message. The PARITY CONTROL signal becomes a high-level to enable control gate A307-U1C. (Refer to paragraph 4-45.) The output of the gate at pin A307-12 is a high-level parity status signal, which is applied to one reset input of the parity error flip flop A307-U1D and U2A at pin A307-2.

4-63. The parity error flip flop A307-U1D and U2A is set 11 times within the data message period by the leading edge of each $\overline{\text{PARITY STROBE}}$ input to the flip flop at pin A307-15. Thus, at the end of the message after

the full 88 bits of data have been examined for parity, the parity error flip flop is set by the 11th $\overline{\text{PARITY STROBE}}$ signal from the parity sample detector A312-U4B. Since the PARITY CONTROL signal that conditions control gate A307-U1C becomes a high level at the first shift clock after the end of message, the parity error flip flop A307-U1D and U2A is in a set condition when the high-level parity status signal from the control gate is applied to the flip flop at pin A307-2.

4-64. The flip flop A307-U1D and U2A can be reset only by a low-level signal. Since the parity status signal input on the reset line from control gate A307-U1C is a high level, the parity error flip flop does not reset. As a result, the output of the flip flop at pin A307-6 is a low-level signal that is inverted by A105-U9A to become a high-level $\overline{\text{PARITY ERROR}}$ at pin A105-7. This high-level $\overline{\text{PARITY ERROR}}$ signal inhibits the PARITY ERROR lamp in the indicator assembly A1A3 of the control panel from lighting. Thus, the examination and detection of correct odd parity is indicated by the PARITY ERROR lamp not lighting.

4-65. If the parity count is incorrect, the parity comparison signals P1 through P8 from the bit parity status checker are not all high levels at the end of the 88-bit data message. The resultant parity status output of the correct parity detector A311-U3A at pin A311-29 is now a high level to be applied to control gate A307-U1C at pin A307-10. As before, the control gate, after the end of the message, is enabled by the high-level PARITY CONTROL input from end of message generator A304-U2A. The output of the gate at pin A307-12 is a low-level parity status signal, which is applied

to the reset input of the already set flip flop A307-U1D and U2A. The flip flop resets, causing the output at pin A307-6 to be a high level signal that is inverted by inverter A105-U9A to become a low-level $\overline{\text{PARITY ERROR}}$ at pin A105-7. This low-level $\overline{\text{PARITY ERROR}}$ signal permits the PARITY ERROR lamp (in OUTPUT display) to light, thereby indicating the examination and detection of an incorrect odd parity count.

4-66. At the start of a new message, a SYNC signal from pin A305-34 of the FSK decoding circuits resets the parity control flip flop A304-U2A in the message/bit counter of the selected message circuits. The PARITY CONTROL output at pin A304-26 now becomes a low level to inhibit control gate A307-U1C in the message parity checker circuits. The parity checking circuits are now held inoperative until the first shift clock after the end of message, at which time the PARITY CONTROL signal goes high to enable the control gate A307-U1C, thereby permitting the message parity checker circuits to function for the check of parity.

4-67. AZIMUTH REGISTER GROUP

4-68. The azimuth positioning the scanning beacon radar antenna of the Video Signal Processor is represented by the logic status of the azimuth position bits AZ0 through AZ11 at MEMORY connector J7 of the test set. These input bits AZ0 through AZ11 are each applied to a corresponding inverter (a gate conditioned by +5 vdc) in the azimuth position gating circuits. These gates are contained on printed circuit cards A106, A107, A203, A205, A206, and A207.

Inverted outputs A0 through A11 appear at pins A207-17, A207-7, A206-17, A206-7, A205-7, A203-17, A203-7, A107-17, A107-7, A106-17, and A106-7, respectively. Any low-level A0 through A11 signal lights a corresponding AZIMUTH REGISTER light-emitting diode in the indicator card assembly A1A8 of the control panel A1. Since the A0 through A11 signals are obtained by inversion of the input position bits AZ0 through AZ11, all lit AZIMUTH REGISTER lamps now represent the scan position of the beacon radar antenna.

4-69. TRANSFER REGISTER GROUP

4-70. The 31 test transfer register signals from the Video Signal Processor are applied as low-level inputs to the test set at connector J6. The test transfer register signals are identified as:

a. $\overline{\text{X1 GARBLE}}$ ($\overline{\text{X1G}}$)

b. $\overline{\text{REPLY}}$ ($\overline{\text{R}}$)

c. $\overline{\text{XITT}}$ ($\overline{\text{TT}}$)

d. $\overline{\text{EMER}}$ ($\overline{\text{E}}$)

e. $\overline{\text{X1SP1}}$ ($\overline{\text{SP1}}$)

f. $\overline{\text{X1R0}}$ ($\overline{\text{R0}}$)

g. $\overline{\text{X1X}}$ ($\overline{\text{X}}$)

h. $\overline{\text{X1R1}}$ through $\overline{\text{X1R12}}$ ($\overline{\text{R1}}$ through $\overline{\text{R12}}$)

i. $\overline{\text{X1A1}}$, $\overline{\text{X1A2}}$, and $\overline{\text{X1A4}}$ ($\overline{\text{A1}}$, $\overline{\text{A2}}$, and $\overline{\text{A4}}$)

j. $\overline{\text{X1B}}$, $\overline{\text{X1B2}}$, and $\overline{\text{X1B4}}$ ($\overline{\text{B1}}$, $\overline{\text{B2}}$, and $\overline{\text{B4}}$)

k. $\overline{\text{X1C1}}$, $\overline{\text{X1C2}}$, and $\overline{\text{X1C4}}$ ($\overline{\text{C1}}$, $\overline{\text{C2}}$, and $\overline{\text{C4}}$)

l. $\overline{\text{X1D1}}$, $\overline{\text{X1D2}}$, and $\overline{\text{X1D4}}$ ($\overline{\text{D1}}$, $\overline{\text{D2}}$, and $\overline{\text{D4}}$)

4-71. These test transfer register signal inputs are applied to corresponding inverters (gates conditioned by +5 vdc) in the transfer register getting circuits contained on printed circuit cards A202 and A204. The inverted outputs are then applied to corresponding inverters (gates similarly conditioned as inverters), on printed circuit cards A203 and A205. Through this double inversion, the low-level test transfer register signal imports are maintained to be the required low levels to light corresponding TRANSFER REGISTER lamps of the indicator lamp assembly A1A9 of control panel A1.

4-72. TARGET AND REPLY REGISTER TRANSFER GROUP

4-73. Target and reply information from the memory registers in the Video Signal Processor are applied on 16 input lines to the test set at MEMORY connector A1J1. Since there can be as much as 128 bits of test target and relay information to be displayed, these bits are time multiplexed onto the 16 input lines to the test set in eight groups of low-level memory bits $\overline{\text{M01}}$ through $\overline{\text{M16}}$. Accompanying these memory inputs at MEMORY connector A1J1 are 10 high-level signals: a target reset, a reply reset, six target transfer strobes, and two reply transfer strobes. Both high-level reset signals are inverted to provide low-level $\overline{\text{TR RESET}}$ and $\overline{\text{RR RESET}}$ signals used to clear all transfer registers in both the memory target transfer control and memory reply transfer control circuits. Whatever memory data bits appear on the 16 test set input lines are applied to all registers, but only those registers which are strobed by a corresponding inverted target or reply transfer strobe input transfer the memory data bits for display in the TARGET REGISTER or REPLY REGISTER display sections

of the control panel. In this manner, the time multiplexed 128 target and reply data bits from the memory registers of the Video Signal Processor are demultiplexed for complete display of all these bits as received in time sequence.

4-74. When the TARGET REGISTER CLEAR and the REPLY REGISTER push-button switches A1S3 and A1S15, respectively, are depressed, ground signals are applied to the Video Signal Processor through pins t and u, respectively, of MEMORY connector A1J7. These ground signals clear the target and reply memory registers in the Video Signal Processor which in turn applies high level target register reset (TR RESET) and reply register reset (RR RESET) signals back to the test set at pin A1J7-P and N, respectively. The TR RESET signal is inverted by inverters A103-U7A and A103-U2B with low-level $\overline{\text{TR RESET}}$ signals appearing at pins A103-10 and 25, respectively. The low-level $\overline{\text{TR RESET}}$ signal at pin A103-25 clears twelve transfer registers A114-U1 through U6 and A314-U1 through U6. The low-level TR RESET signal at pin A103-10 clears the remaining twelve trasfer registers A113-U1 through U6 and A313-U1 through U6. Similarly, the $\overline{\text{RR RESET}}$ signal input is inverted by inverter A103-U3A with a low-level $\overline{\text{RR RESET}}$ signal output at pin A103-18. This low-level $\overline{\text{RR RESET}}$ signal clears all twelve reply transfer registers A101-U1 through U6 and A201-U1 through U6.

4-75. As noted, the Q6 target bits and 32 reply bits are time multiplexed, in eight groups, onto 16 input lines as the low-level $\overline{M01}$ through $\overline{M06}$ signals. Each multiplexed group of 16 bits are applied at pins A102-31, 29, 23, 21, 39, 37, 8, 4, 14, 16, 20, 26, 38, 36, 24, and 2, respectively, to corresponding inverters contained on printed circuit card A102. The resultant high-level M01 through M16 outputs of these inverters are applied to all 4-bit latch transfer registers contained on printed circuit cards A113, A114, A313, A314, A101, and A201.

4-76. Demultiplexing is accomplished when one of the eight high-level TRX1 through TRX6, RRX1, and RRX2 signal inputs from the Video Signal Processor corresponding to the particular group of input bits $\overline{M01}$ through $\overline{M16}$ is received at the test set. Time strokes TRX1 through TRX6, when received, are applied from MEMORY connector A1J7 to pins A103-31, 29, 21, 39, 37, and 4, respectively, of inverters contained on printed circuit card A103. The respective low-level $\overline{TRX1}$ through $\overline{TRX6}$ outputs at pins A103-33, 27, 19, 41, 35, and 6 are used to stroke the M01 through M16 data bits out of corresponding target transfer registers as listed in table 4-1. Similarly, time strokes RRX1 and RRX2, when received, are applied from MEMORY connector A1J7 to pins A103-14 and 20, of inverters A103-U5A and A103-U2B, respectively. The low-level $\overline{RRX1}$ and $\overline{RRX2}$ outputs at pins A103-12 and 22, respectively are used to stroke the M01 through M16 data bits out of corresponding reply transfer registers as listed in table 4-1. (Refer to figure 4-5 for timing sequence of the six target transfer stroke inputs TRX1 through TRX6 and the two reply transfer strobe inputs RRX1 and RRX6.)

Table 4-1. Transfer Register Strobing

Transfer Strobe	Transfer Register Strobed	Test Information $\overline{M01}$ through $\overline{M16}$ Inputs
$\overline{TRX1}$	A114-U1, U4 and A314-U1, U4	Target range and control
$\overline{TRX2}$	A114-U2, U5 and A314-U2, U5	Target azimuth and control
$\overline{TRX3}$	A114-U3, U6 and A314-U3, U6	Target mode 1 or 2
$\overline{TRX4}$	A113-U1, U4 and A313-U1, U4	Target mode 2 or 3/A
$\overline{TRX5}$	A113-U2, U5 and A313-U2, U5	Target mode C
$\overline{TRX6}$	A113-U3, U6 and A313-U3, U6	Target mode C
$\overline{RRX1}$	A101-U1, U2 and A201-U1, U2	Relay range and control
$\overline{RRX2}$	A101-U3, U4 and A201-U3, U4	Reply code and control

4-77. When strobed by the proper target or reply transfer strobe signal, the transfer registers output the applicable stored high-level M01 through M16 signals to corresponding gates, conditioned as inverters, on printed circuit cards A104, A109, A111, A112, A209, A211, A212, and A213. The low-level outputs of these inverters represent the target or reply information associated with the transfer register being strobed (see table 4-1), and are applied to light the corresponding TARGET REGISTER or REPLY REGISTER display lamps contained on indicator card assemblies, A1A4, A1A5, A1A6, and A1A7 of control panel A1.

4-78. POWER DISTRIBUTION CIRCUITS.

4-79. Primary 115-volts ac power can be applied to the test set either at power connector A1J1 on the front control panel or at the rear connector J8. Selection

of the connector to be used is made by setting of control panel switch S14. The 115-volt ac primary power at the front connector A1J1 is applied through the filters FL1 and FL2 (rf decouplers) to switch S14 terminals 3 and 6. However, the 115-volts ac primary power at the rear connector J8 is applied directly to switch S14 terminals 1 and 4 without initial rf filters. From switch S14 the 115-volts ac is applied through another pair of rf filters FL3 and FL4 to POWER switch A1S1 on the control panel. When the switch A1S1 is set to ON, the primary power is applied through fuse A1F1 to terminal board A2TB1-1 and 2 to light POWER lamp DS1, turn on blower B1, and is ac input to power supply PS1. The power supply PS1 is an hermetically sealed unit that supplies +5 volts dc to terminal 7 of terminal board A2TB1 for distribution to the printed circuit cards of the test set and to LAMP TEST switch A1S2. When the LAMP TEST switch is not depressed, +5 volts dc is applied through normally closed contacts 1 and 2 to pin 43 of each of the following printed circuit cards: A102, A103, A104, A105, A106, A109, A111, A112; A205, A206, A207, A211, A213; and A310. When LAMP TEST switch is depressed, a ground signal is applied through closed contacts 3 and 4 to terminal E32 of each of the following indicator lamp assemblies, thereby testing the light emitting diodes on these assemblies: A1A1, A1A2, A1A4, and A1A5 thru A1A9. Direct distribution of +5 volts dc from terminal board A2TB1-1 and 2 is made to pin 43 of printed circuit cards A101, A110, A201, A301, and A309.

4-80. MANUAL CLEARING AND MONITORING CIRCUITS.

4-81. The test set control panel A1 contains four CLEAR pushbutton switches: TARGET REGISTER A1S3, REPLY REGISTER A1S15, AZIMUTH REGISTER A1S13, and TRANSFER REGISTER A1S4. When each of these switches is depressed, a ground signal is applied to pins t, u, v, and w, respectively, of MEMORY connector A1J7 to serve as a clearing or reset signal to the corresponding register in the Video Signal Processor. Two major input signals, $\overline{\text{TRU OUTPUT}}$ and $\overline{\text{TRU START}}$, from the Video Signal Processor are applied to connector A1J6 at pins k and j, respectively. These signals are applied to the FSK decoding and selected message circuits of the test set and are also applied to inverters A310-U5A and A310-U3A, respectively. The inverted output TRU OUTPUT at pin A310-12 is applied to TRU OUTPUT coaxial connector A1J3 on the control panel for external oscilloscope monitoring purposes. The inverted output TRU START at pin A310-18 is applied to TRU START coaxial connector A1J2 for monitoring purposes. A third major signal, $\overline{\text{MAIN GATE}}$, from the Video Signal Processor is applied to the test set at pin m of connector A1J6. This $\overline{\text{MAIN GATE}}$ signal input is not used by the major circuits of the test set. However, the $\overline{\text{MAIN GATE}}$ signal is inverted by inverter A310-U with the inverted MAIN GATE at pin A310-32 applied to MAIN GATE coaxial connector A1J4 for monitoring purposes.

CHAPTER 5

MAINTENANCE

5-1. INTRODUCTION. This chapter contains maintenance instructions for the Video Signal Processor Test Set AN/TPM-32. Section I contains the organizational/field maintenance instructions and alignment and adjustment procedures. Section II references the special maintenance instructions given in the Electronics Circuit Plug-In Test Set, T.O. 33D7-49-55-2, and the Power Supply Test Set, T.O. 33D7-6-24-2.

SECTION I

ORGANIZATION/FIELD MAINTENANCE

5-2. SCOPE.

5-3. This section provides instructions for maintenance of the test set on an organizational/field maintenance level. Component board and subassembly performance tests and fault isolation procedures are provided to enable circuit testing and fault isolation to a circuit card, group of circuit cards, power supply subassembly, or front panel control or indicator.

5-4. After the suspect circuit card is removed from the test set, it is further tested by the Electronic Circuit Plug-In Test Set AN/TPM-36 (T.O. 33D7-49-55-2). When a suspect power supply is removed from the test set, it is further tested by the Power Supply Test Set AN/TPM-37 (T.O. 33D7-6-24-2).

5-5. MAINTENANCE TEST EQUIPMENT.

5-6. Table 5-1 lists the test equipment required for organizational/field maintenance and gives a brief description of each.

5-7. TEST POINTS.

5-8. Table 5-2 lists the location and function of all test points used for maintenance performance tests and fault isolation procedures. The circuit function column gives the signal observed or the test being made at the test point location.

Table 5-1. Maintenance Test Equipment

TEST EQUIPMENT	CHARACTERISTICS
Pulse Generator SG-816	Repetition Rate: 0 to 1 MHz Pulse Width: 30 nanosec to 10 milli sec. Amplitude: 0 to 20 volts (+ or - polarity) Synchronization: input - 2 volts delay - variable from 50 nanosec to 20 milli sec. Trigger: external or manual, one shot
Multimeter AN/PSM-6	Voltage: 0 to 500 V ±5% DC and AC, 60 Hz and 400 Hz Resistance: 1 ohm to 1 megohm ±10%

Table 5-1. Maintenance Test Equipment (Cont)

TEST EQUIPMENT	CHARACTERISTICS
Oscilloscope AN/USM-281	Vertical Amplifier (dual trace) bandwidth: 50 MHz rise time: 7.5 nanosec. input resistance: 1 megohm calibrated deflection factor: 50 milli volts/cm to 10 v/cm Horizontal Amplifier (dual sweep) time base: 12.5 nanosec/cm to 1 sec/cm calibrated sweep delay: 200 nano-seconds to 1 second jitter: 1 nanosecond input power: 115 vac 60 Hz and 400 Hz

Table 5-2. Test Points

TEST POINT	LOCATION	FUNCTION
E41	Terminal board	Continuity check
E42	Terminal board	Continuity check
E43	Terminal board	Continuity check
E44	Terminal board	Continuity check
E6-E12	Terminal board	Continuity check

Table 5-2. Test Points (Cont)

TEST POINT	LOCATION	FUNCTION
J2	TRU START on front panel	Square wave
J3	TRU START on front panel	Square wave
J4	MAIN GATE on front panel	Square wave
TB1-7	PS1	+5V
TP3	A1PS1	+5V
XA303 pin 31	Circuit card connector	10.356 MHz
XA304 pin 10	Circuit card connector	Pulse burst
XA304 pin 13	Circuit card connector	Pulse burst
XA304 pin 25	Circuit card connector	Logic 0
XA304 pin 20	Circuit card connector	$\overline{\text{GO - SYNC}}$
XA304 pin 25	Circuit card connector	Logic 0
XA305 pin 30	Circuit card connector	Serial data
XA305 pin 24	Circuit card connector	5.178 MHz clock
XA305 pin 14	Circuit card connector	Shift clock
XA305 pin 34	Circuit card connector	SYNC
XA305 pin 38	Circuit card connector	STROBE
XA306 pin 25	Circuit card connector	Logic 0
XA306 pin 18	Circuit card connector	Shift clock
XA307 pin 6	Circuit card connector	Logic 1

Table 5-2. Test Points (Cont)

TEST POINT	LOCATION	FUNCTION
XA307 pin 20	Circuit card connector	Logic 0
XA308 pin 2	Circuit card connector	Shift clock
XA310 pin 1	Circuit card connector	Parity strobe
XA310 pin 2	Circuit card connector	Parity strobe
XA310 pin 22	Circuit card connector	Shift
XA311 pin 29	Circuit card connector	Pulse burst
XA311 pin 31	Circuit card connector	Pulse burst or square wave
XA311 pin 29	Circuit card connector	Logic 0 or pulse burst
XA311 pins 32, 30, 28, 26, 27, 25, 23, 21	Circuit card connector	Logic 1
XA312 pin 1	Circuit card connector	Logic 1
XA312 pin 9	Circuit card connector	$\overline{\text{SYNC}}$
XA312 pin 36	Circuit card connector	$\overline{\text{BC 4}}$

5-9. PERFORMANCE TEST AND FAULT ISOLATION PROCEDURES.

5-10. To facilitate performance testing, and fault isolation, a diagnostic flow chart based on the maximum use of circuit functions in a minimum number of steps is provided in figure 5-1. The diagnostic flow chart contains instructions within blocks connected by GO-path lines to provide a complete checkout of the Video Signal Processor. Instructions with blocks

connected by NO-GO path lines provide fault isolation procedures. The procedures exercise all built-in test functions first, since these rapidly provide a status indication and exercise those circuits which have the highest probability of failure. Then, progressively lesser circuit functions are tested.

5-11. COMPLETE PERFORMANCE TEST.

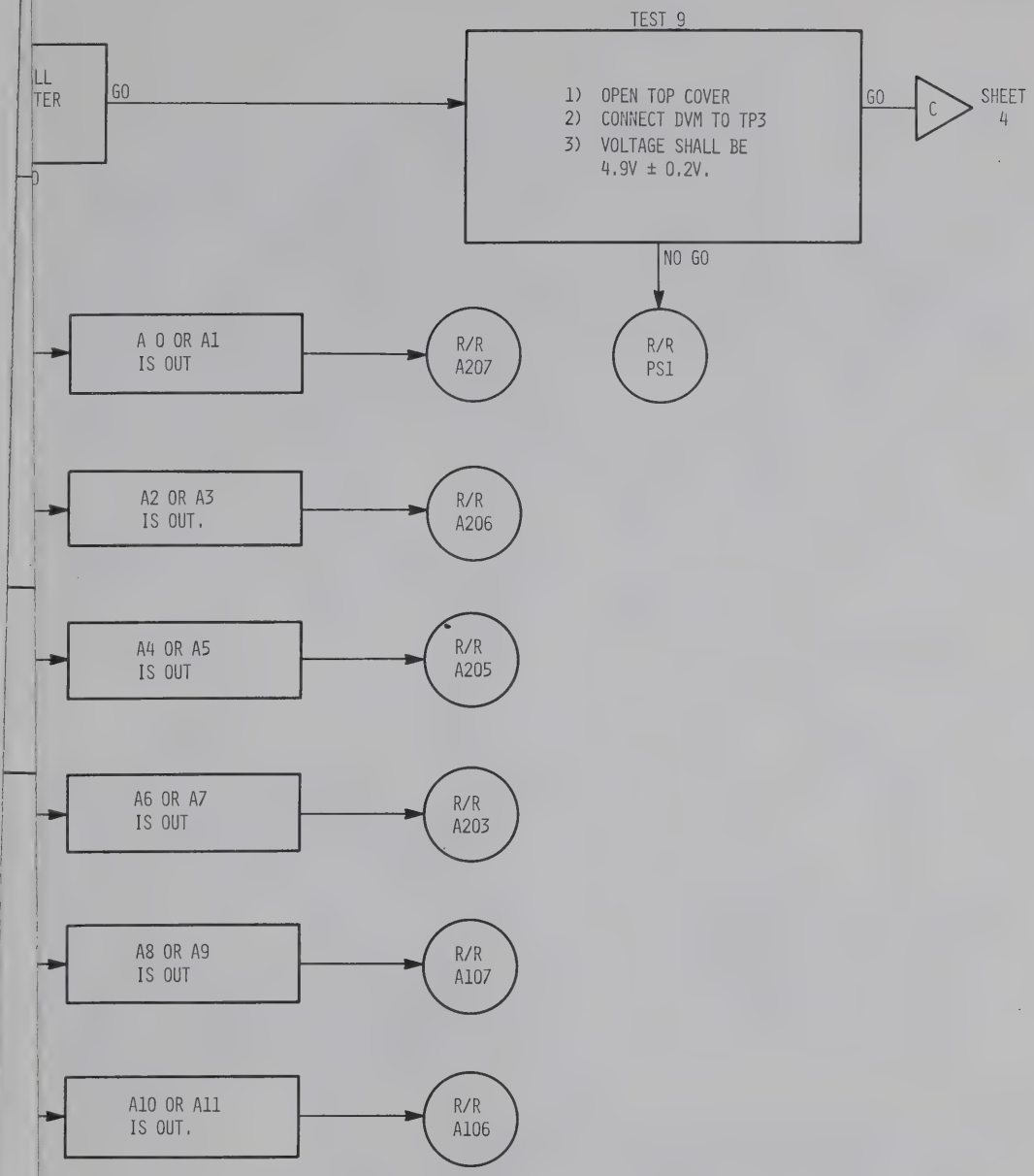
5-12. A performance test is required when major circuit function repairs have been accomplished or if a complete checkout is desired. Perform this test by executing all the tests along the GO path lines of the diagnostic flow chart (figure 5-1).

5-13. HOW TO USE THE DIAGNOSTIC FLOW CHART.

5-14. FAULT ISOLATION. Before attempting fault isolation procedures, the technician should become familiar with the structure of the diagnostic, its limitations, and the tests and test equipment required.

5-15. Since the fault isolation procedures are based on the process of elimination, each step of the instruction must be followed without skipping until the malfunction is isolated.

5-16. As system circuit functions and fault isolation procedures become fully understood, the diagnostic may be entered at points based on observed symptoms, rather than the beginning. Make certain, however, that all test setups are correct. After the fault is isolated and the repair is made, the entire performance test should be performed.



A61036-11-3

FIGURE 5-1. PERFORMANCE TESTS AND FAULT ISOLATION PROCEDURES FLOW DIAGRAM (SHEET 3 OF 17)

connected by NO-GO path lines provide fault isolation procedures. The procedures exercise all built-in test functions first, since these rapidly provide a status indication and exercise those circuits which have the highest probability of failure. Then, progressively lesser circuit functions are tested.

5-11. COMPLETE PERFORMANCE TEST.

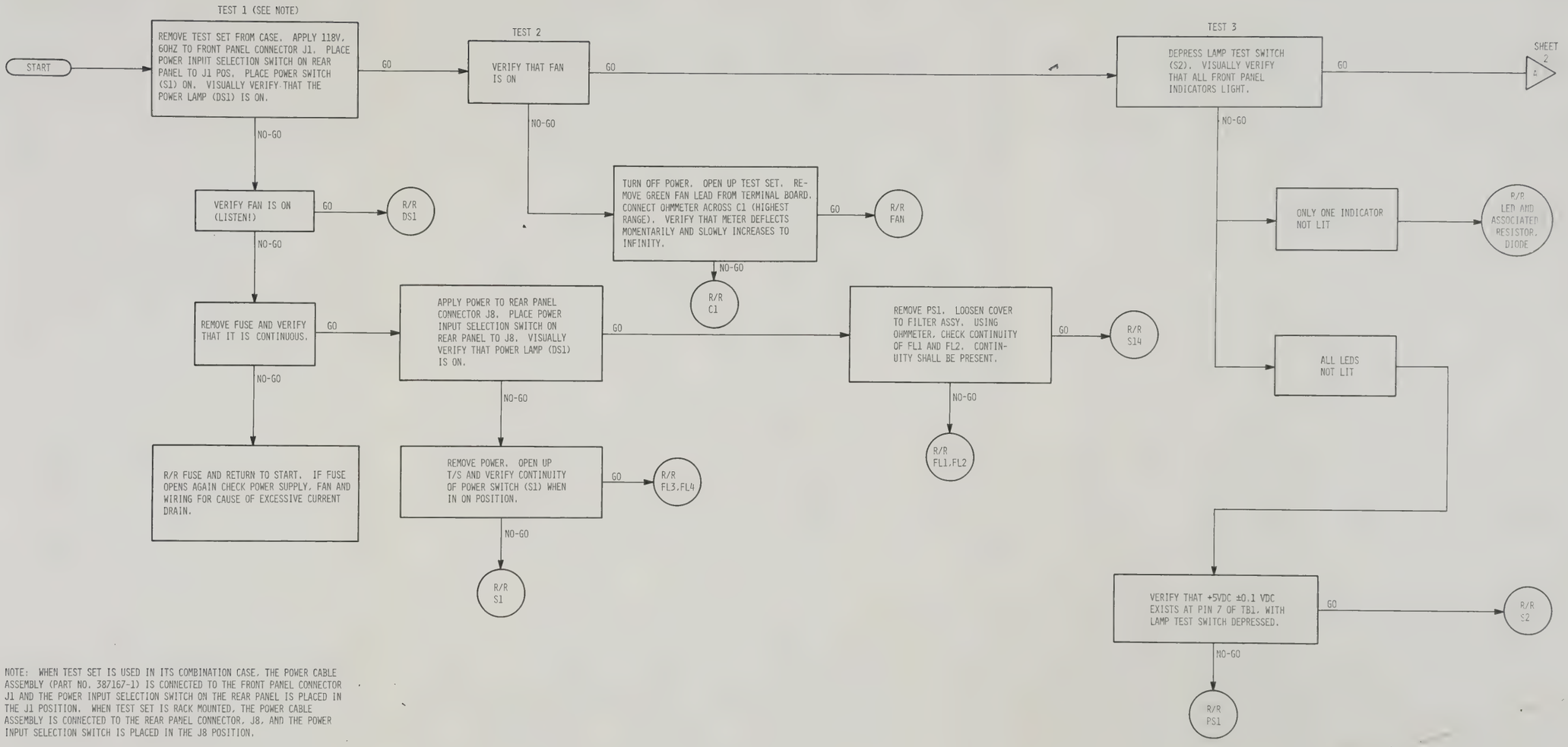
5-12. A performance test is required when major circuit function repairs have been accomplished or if a complete checkout is desired. Perform this test by executing all the tests along the GO path lines of the diagnostic flow chart (figure 5-1).

5-13. HOW TO USE THE DIAGNOSTIC FLOW CHART.

5-14. FAULT ISOLATION. Before attempting fault isolation procedures, the technician should become familiar with the structure of the diagnostic, its limitations, and the tests and test equipment required.

5-15. Since the fault isolation procedures are based on the process of elimination, each step of the instruction must be followed without skipping until the malfunction is isolated.

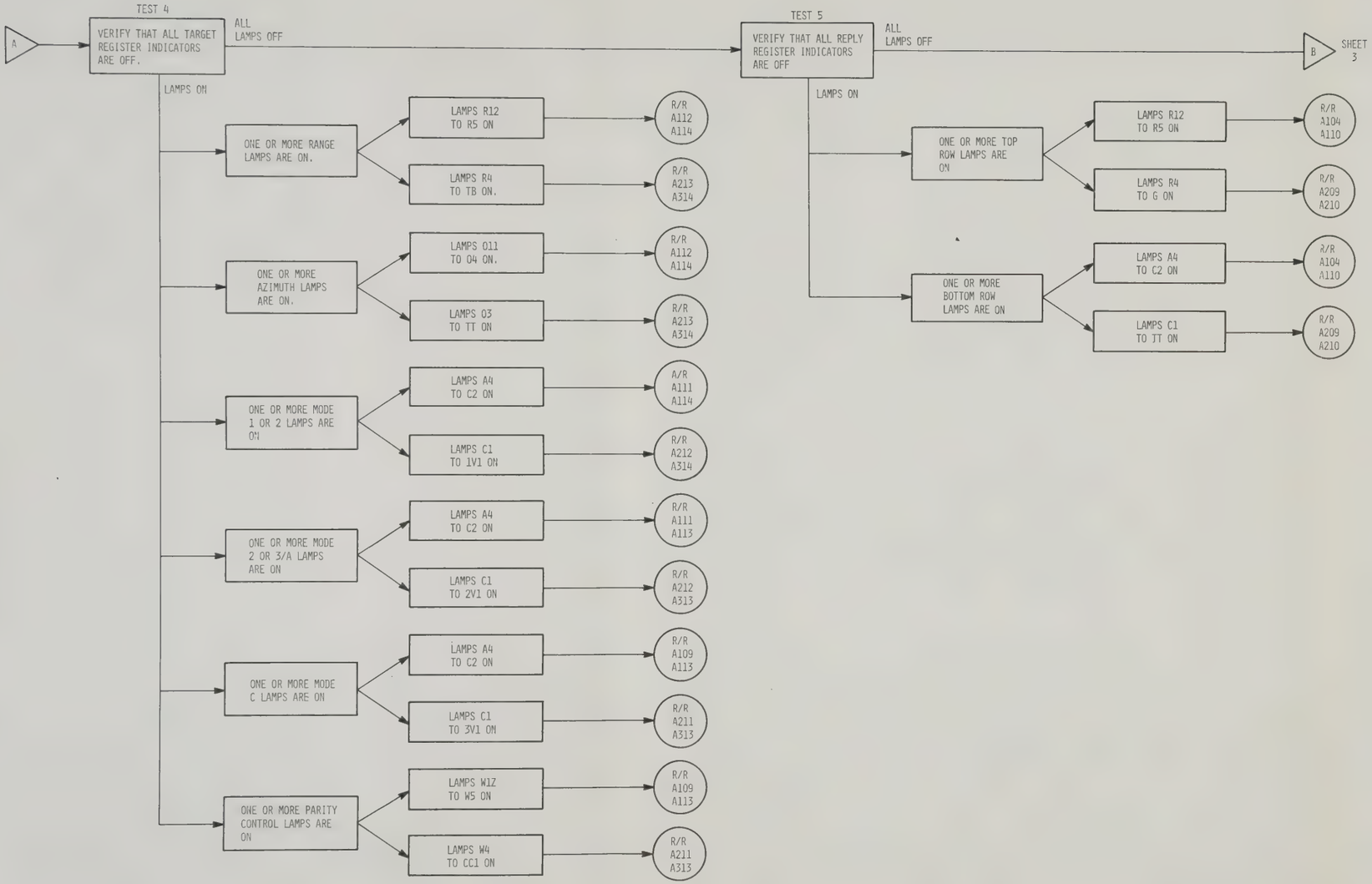
5-16. As system circuit functions and fault isolation procedures become fully understood, the diagnostic may be entered at points based on observed symptoms, rather than the beginning. Make certain, however, that all test setups are correct. After the fault is isolated and the repair is made, the entire performance test should be performed.


TEST 1 (SEE NOTE)
START
REMOVE TEST SET FROM CASE. APPLY 118V, 60HZ TO FRONT PANEL CONNECTOR J1. PLACE POWER INPUT SELECTION SWITCH ON REAR PANEL TO J1 POS. PLACE POWER SWITCH (S1) ON. VISUALLY VERIFY THAT THE POWER LAMP (DS1) IS ON.
GO
NO-GO
TEST 2
VERIFY THAT FAN IS ON
GO
NO-GO
TEST 3
DEPRESS LAMP TEST SWITCH (S2). VISUALLY VERIFY THAT ALL FRONT PANEL INDICATORS LIGHT.
GO
SHEET 2
NO-GO
VERIFY FAN IS ON (LISTEN!)
GO
R/R DS1
NO-GO
TURN OFF POWER. OPEN UP TEST SET. REMOVE GREEN FAN LEAD FROM TERMINAL BOARD. CONNECT OHMMETER ACROSS C1 (HIGHEST RANGE). VERIFY THAT METER DEFLECTS MOMENTARILY AND SLOWLY INCREASES TO INFINITY.
GO
R/R FAN
NO-GO
R/R C1
ONLY ONE INDICATOR NOT LIT
R/R LED AND ASSOCIATED RESISTOR, DIODE
REMOVE FUSE AND VERIFY THAT IT IS CONTINUOUS.
GO
NO-GO
APPLY POWER TO REAR PANEL CONNECTOR J8. PLACE POWER INPUT SELECTION SWITCH ON REAR PANEL TO J8. VISUALLY VERIFY THAT POWER LAMP (DS1) IS ON.
GO
NO-GO
REMOVE PS1. LOOSEN COVER TO FILTER ASSY. USING OHMMETER, CHECK CONTINUITY OF FL1 AND FL2. CONTINUITY SHALL BE PRESENT.
GO
R/R S14
NO-GO
R/R FL1,FL2
ALL LEDS NOT LIT
R/R FUSE AND RETURN TO START. IF FUSE OPENS AGAIN CHECK POWER SUPPLY, FAN AND WIRING FOR CAUSE OF EXCESSIVE CURRENT DRAIN.
REMOVE POWER. OPEN UP T/S AND VERIFY CONTINUITY OF POWER SWITCH (S1) WHEN IN ON POSITION.
GO
R/R FL3,FL4
NO-GO
R/R S1
VERIFY THAT +5VDC ±0.1 VDC EXISTS AT PIN 7 OF TB1, WITH LAMP TEST SWITCH DEPRESSED.
GO
R/R S2
NO-GO
R/R PS1

NOTE: WHEN TEST SET IS USED IN ITS COMBINATION CASE, THE POWER CABLE ASSEMBLY (PART NO. 387167-1) IS CONNECTED TO THE FRONT PANEL CONNECTOR J1 AND THE POWER INPUT SELECTION SWITCH ON THE REAR PANEL IS PLACED IN THE J1 POSITION. WHEN TEST SET IS RACK MOUNTED, THE POWER CABLE ASSEMBLY IS CONNECTED TO THE REAR PANEL CONNECTOR, J8, AND THE POWER INPUT SELECTION SWITCH IS PLACED IN THE J8 POSITION.

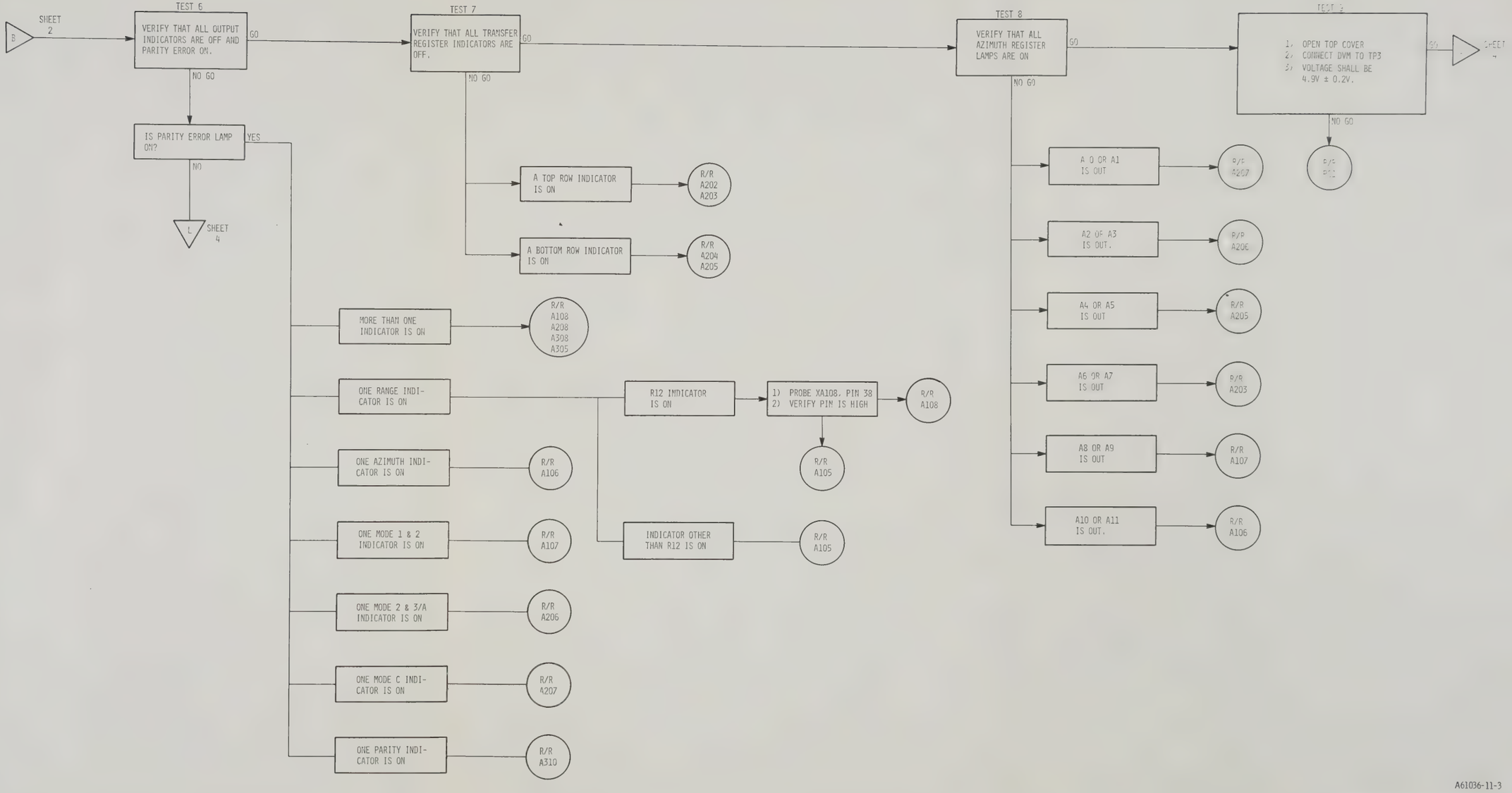
A61036-11-1

FIGURE 5-1. PERFORMANCE TESTS AND FAULT ISOLATION PROCEDURES FLOW DIAGRAM (SHEET 1 OF 17)


A
TEST 4
VERIFY THAT ALL TARGET REGISTER INDICATORS ARE OFF.
ALL LAMPS OFF
LAMPS ON
ONE OR MORE RANGE LAMPS ARE ON.
LAMPS R12 TO R5 ON
LAMPS R4 TO TB ON.
R/R A112 A114
R/R A213 A314
ONE OR MORE AZIMUTH LAMPS ARE ON.
LAMPS O11 TO O4 ON.
LAMPS O3 TO TT ON
R/R A112 A114
R/R A213 A314
ONE OR MORE MODE 1 OR 2 LAMPS ARE ON
LAMPS A4 TO C2 ON
LAMPS C1 TO 1V1 ON
R/R A111 A114
R/R A212 A314
ONE OR MORE MODE 2 OR 3/A LAMPS ARE ON
LAMPS A4 TO C2 ON
LAMPS C1 TO 2V1 ON
R/R A111 A113
R/R A212 A313
ONE OR MORE MODE C LAMPS ARE ON
LAMPS A4 TO C2 ON
LAMPS C1 TO 3V1 ON
R/R A109 A113
R/R A211 A313
ONE OR MORE PARITY CONTROL LAMPS ARE ON
LAMPS W1Z TO W5 ON
LAMPS W4 TO CC1 ON
R/R A109 A113
R/R A211 A313
TEST 5
VERIFY THAT ALL REPLY REGISTER INDICATORS ARE OFF
ALL LAMPS OFF
B
SHEET 3
LAMPS ON
ONE OR MORE TOP ROW LAMPS ARE ON
LAMPS R12 TO R5 ON
LAMPS R4 TO G ON
R/R A104 A110
R/R A209 A210
ONE OR MORE BOTTOM ROW LAMPS ARE ON
LAMPS A4 TO C2 ON
LAMPS C1 TO JT ON
R/R A104 A110
R/R A209 A210

A61036-11-2

FIGURE 5-1. PERFORMANCE TESTS AND FAULT ISOLATION PROCEDURES FLOW DIAGRAM (SHEET 2 OF 17)



A61036-11-3

FIGURE 5-1. PERFORMANCE TESTS AND FAULT ISOLATION PROCEDURES FLOW DIAGRAM (SHEET 3 OF 17)

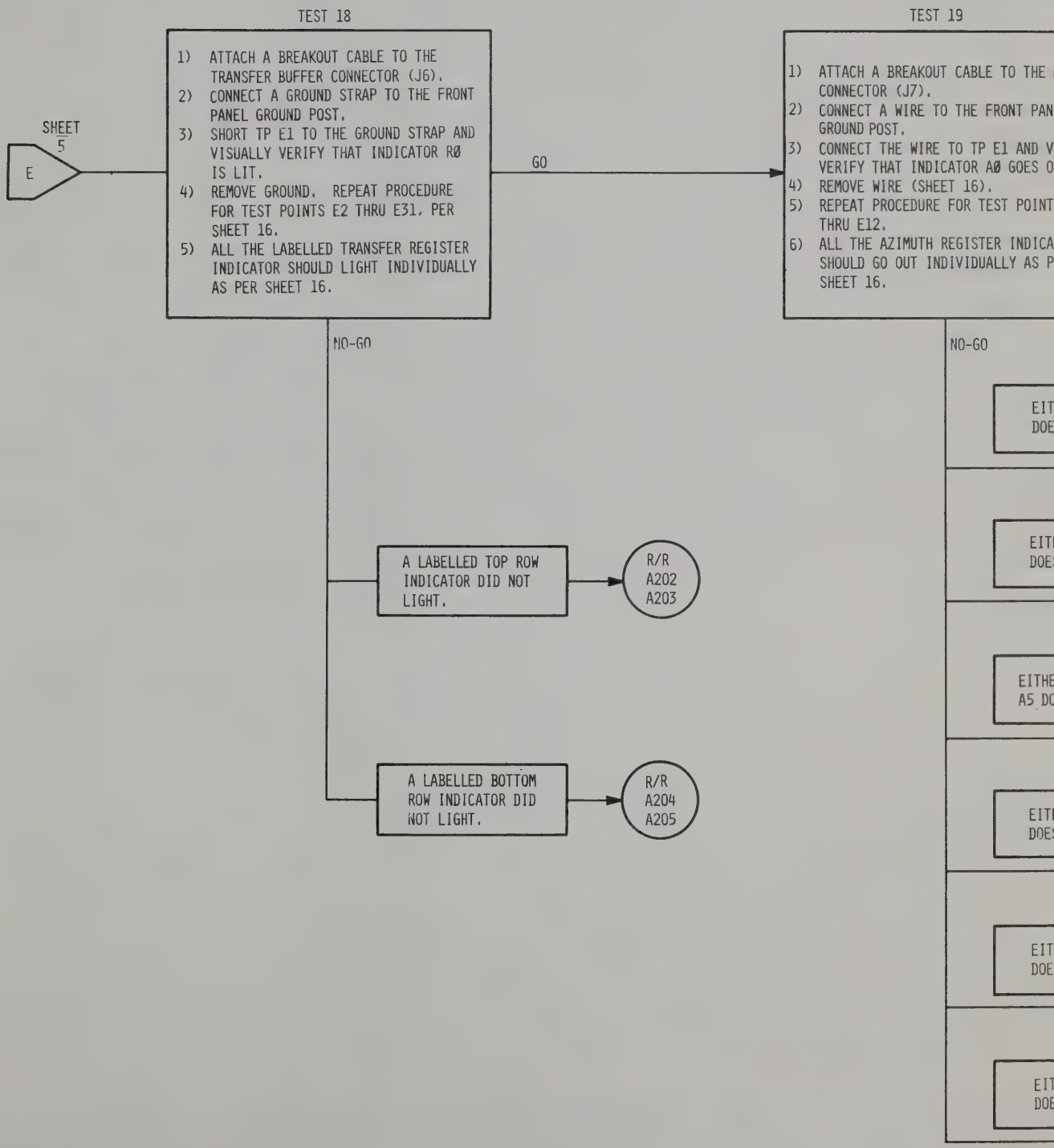
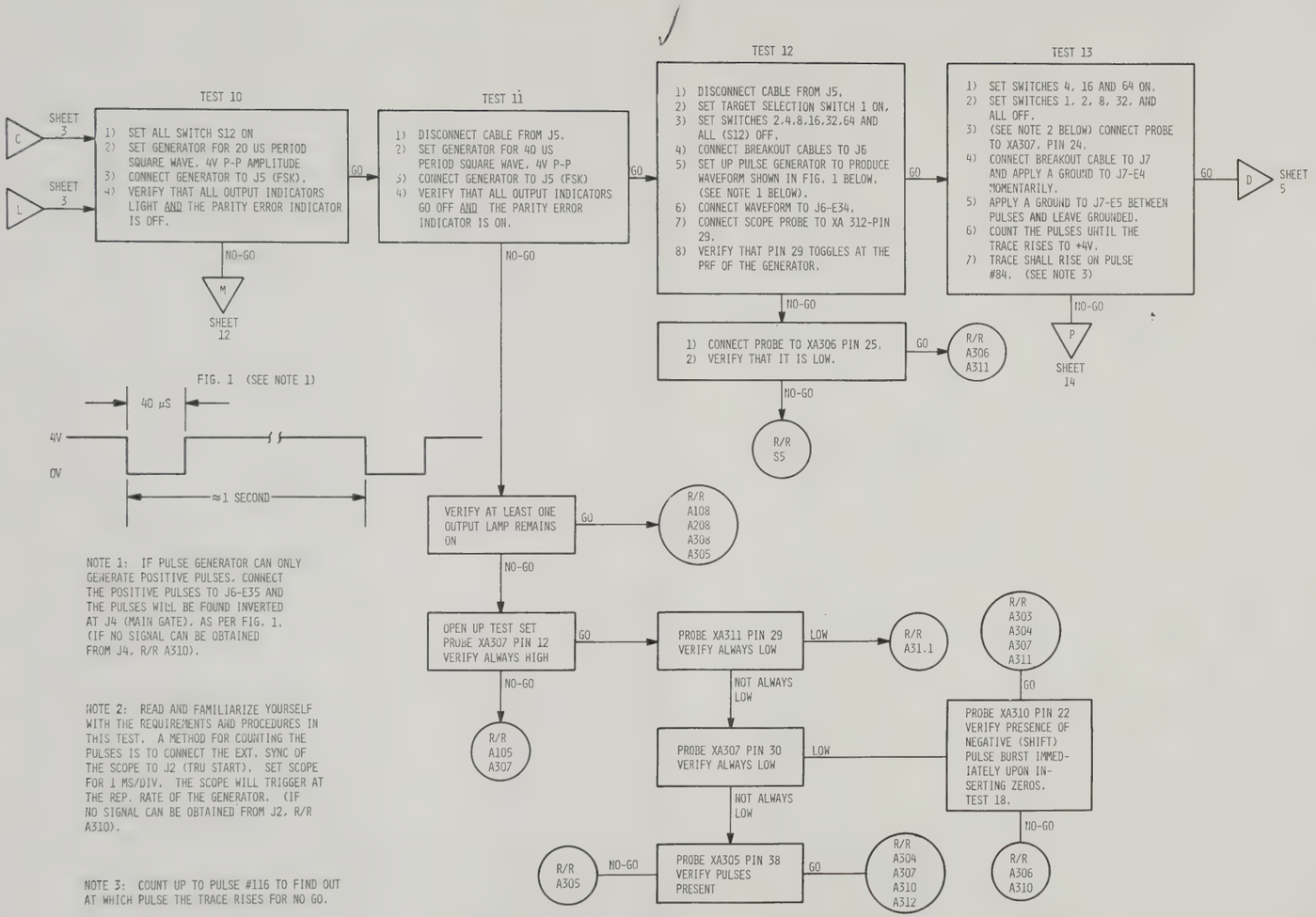
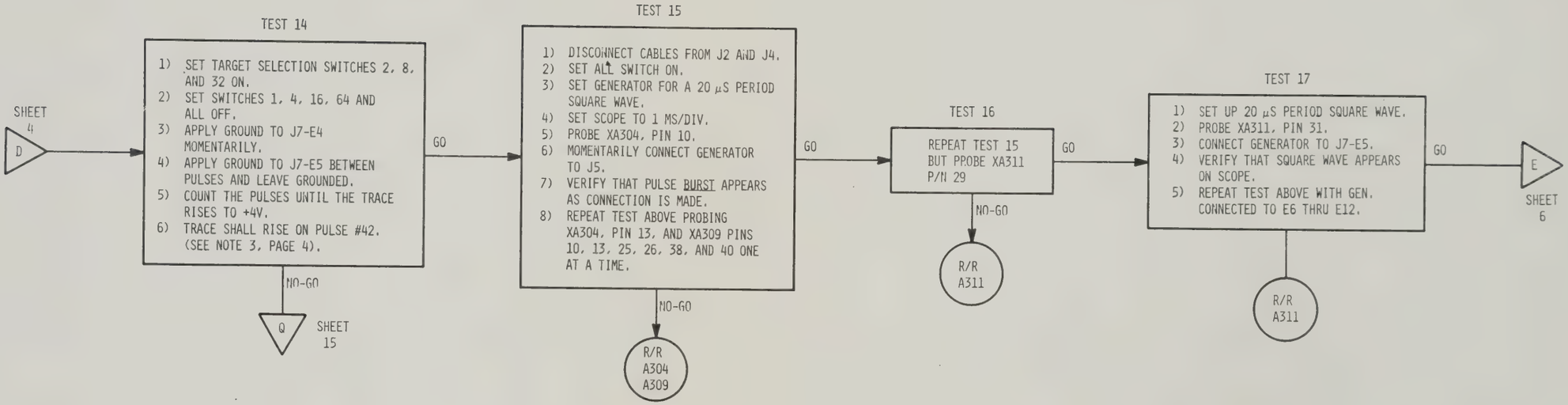

TEST 18
1) ATTACH A BREAKOUT CABLE TO THE TRANSFER BUFFER CONNECTOR (J6).
2) CONNECT A GROUND STRAP TO THE FRONT PANEL GROUND POST.
3) SHORT TP E1 TO THE GROUND STRAP AND VISUALLY VERIFY THAT INDICATOR RØ IS LIT.
4) REMOVE GROUND. REPEAT PROCEDURE FOR TEST POINTS E2 THRU E31, PER SHEET 16.
5) ALL THE LABELLED TRANSFER REGISTER INDICATOR SHOULD LIGHT INDIVIDUALLY AS PER SHEET 16.
SHEET 5
E
GO
TEST 19
1) ATTACH A BREAKOUT CABLE TO THE
CONNECTOR (J7).
2) CONNECT A WIRE TO THE FRONT PAN
GROUND POST.
3) CONNECT THE WIRE TO TP E1 AND V
VERIFY THAT INDICATOR AØ GOES O
4) REMOVE WIRE (SHEET 16).
5) REPEAT PROCEDURE FOR TEST POINT
THRU E12.
6) ALL THE AZIMUTH REGISTER INDICA
SHOULD GO OUT INDIVIDUALLY AS P
SHEET 16.
NO-GO
A LABELLED TOP ROW INDICATOR DID NOT LIGHT.
R/R A202 A203
A LABELLED BOTTOM ROW INDICATOR DID NOT LIGHT.
R/R A204 A205
NO-GO

FIGURE 5-1. PERFORMANCE TESTS AND FAULT ISOLATION PROCEDURES FLOW DIAGRAM (SHEET 6 OF 17)


TEST 10
1) SET ALL SWITCH S12 ON
2) SET GENERATOR FOR 20 US PERIOD SQUARE WAVE, 4V P-P AMPLITUDE
3) CONNECT GENERATOR TO J5 (FSK).
4) VERIFY THAT ALL OUTPUT INDICATORS LIGHT AND THE PARITY ERROR INDICATOR IS OFF.
SHEET 3
C
SHEET 3
L
GO
NO-GO
M
SHEET 12
TEST 11
1) DISCONNECT CABLE FROM J5.
2) SET GENERATOR FOR 40 US PERIOD SQUARE WAVE, 4V P-P
3) CONNECT GENERATOR TO J5 (FSK)
4) VERIFY THAT ALL OUTPUT INDICATORS GO OFF AND THE PARITY ERROR INDICATOR IS ON.
GO
NO-GO
TEST 12
1) DISCONNECT CABLE FROM J5.
2) SET TARGET SELECTION SWITCH 1 ON.
3) SET SWITCHES 2,4,8,16,32,64 AND ALL (S12) OFF.
4) CONNECT BREAKOUT CABLES TO J6
5) SET UP PULSE GENERATOR TO PRODUCE WAVEFORM SHOWN IN FIG. 1 BELOW. (SEE NOTE 1 BELOW).
6) CONNECT WAVEFORM TO J6-E34.
7) CONNECT SCOPE PROBE TO XA 312-PIN 29.
8) VERIFY THAT PIN 29 TOGGLES AT THE PRF OF THE GENERATOR.
GO
NO-GO
TEST 13
1) SET SWITCHES 4, 16 AND 64 ON.
2) SET SWITCHES 1, 2, 8, 32, AND ALL OFF.
3) (SEE NOTE 2 BELOW) CONNECT PROBE TO XA307, PIN 24.
4) CONNECT BREAKOUT CABLE TO J7 AND APPLY A GROUND TO J7-E4 MOMENTARILY.
5) APPLY A GROUND TO J7-E5 BETWEEN PULSES AND LEAVE GROUNDED.
6) COUNT THE PULSES UNTIL THE TRACE RISES TO +4V.
7) TRACE SHALL RISE ON PULSE #84. (SEE NOTE 3)
GO
D
SHEET 5
NO-GO
P
SHEET 14
1) CONNECT PROBE TO XA306 PIN 25.
2) VERIFY THAT IT IS LOW.
GO
R/R A306 A311
NO-GO
R/R S5
FIG. 1 (SEE NOTE 1)
40 µS
4V
0V
≈1 SECOND
VERIFY AT LEAST ONE OUTPUT LAMP REMAINS ON
GO
R/R A108 A208 A308 A305
NO-GO
OPEN UP TEST SET PROBE XA307 PIN 12 VERIFY ALWAYS HIGH
GO
NO-GO
R/R A105 A307
PROBE XA311 PIN 29 VERIFY ALWAYS LOW
LOW
R/R A31.1
NOT ALWAYS LOW
R/R A303 A304 A307 A311
GO
PROBE XA310 PIN 22 VERIFY PRESENCE OF NEGATIVE (SHIFT) PULSE BURST IMMEDIATELY UPON INSERTING ZEROS. TEST 18.
NO-GO
R/R A306 A310
PROBE XA307 PIN 30 VERIFY ALWAYS LOW
LOW
NOT ALWAYS LOW
R/R A305
NO-GO
PROBE XA305 PIN 38 VERIFY PULSES PRESENT
GO
R/R A304 A307 A310 A312
NOTE 1: IF PULSE GENERATOR CAN ONLY GENERATE POSITIVE PULSES, CONNECT THE POSITIVE PULSES TO J6-E35 AND THE PULSES WILL BE FOUND INVERTED AT J4 (MAIN GATE), AS PER FIG. 1. (IF NO SIGNAL CAN BE OBTAINED FROM J4, R/R A310).
NOTE 2: READ AND FAMILIARIZE YOURSELF WITH THE REQUIREMENTS AND PROCEDURES IN THIS TEST. A METHOD FOR COUNTING THE PULSES IS TO CONNECT THE EXT. SYNC OF THE SCOPE TO J2 (TRU START). SET SCOPE FOR 1 MS/DIV. THE SCOPE WILL TRIGGER AT THE REP. RATE OF THE GENERATOR. (IF NO SIGNAL CAN BE OBTAINED FROM J2, R/R A310).
NOTE 3: COUNT UP TO PULSE #116 TO FIND OUT AT WHICH PULSE THE TRACE RISES FOR NO GO.

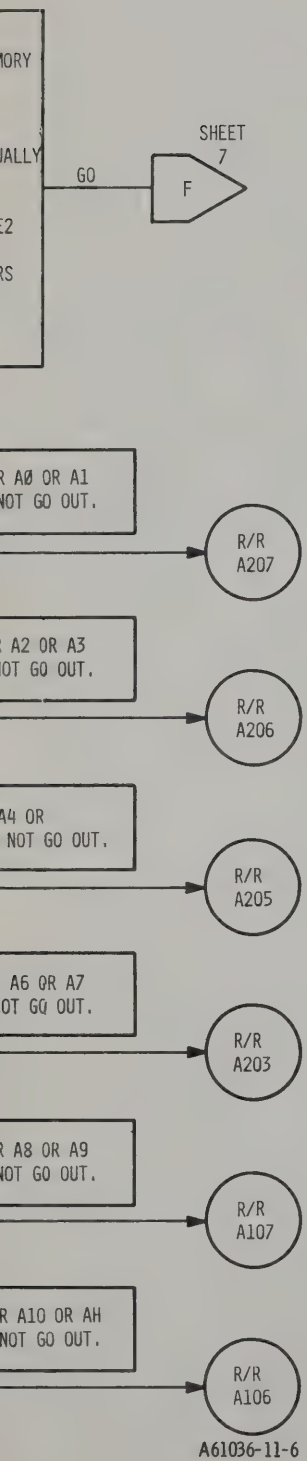
A61036-11-4

FIGURE 5-1. PERFORMANCE TESTS AND FAULT ISOLATION PROCEDURES FLOW DIAGRAM (SHEET 4 OF 17)

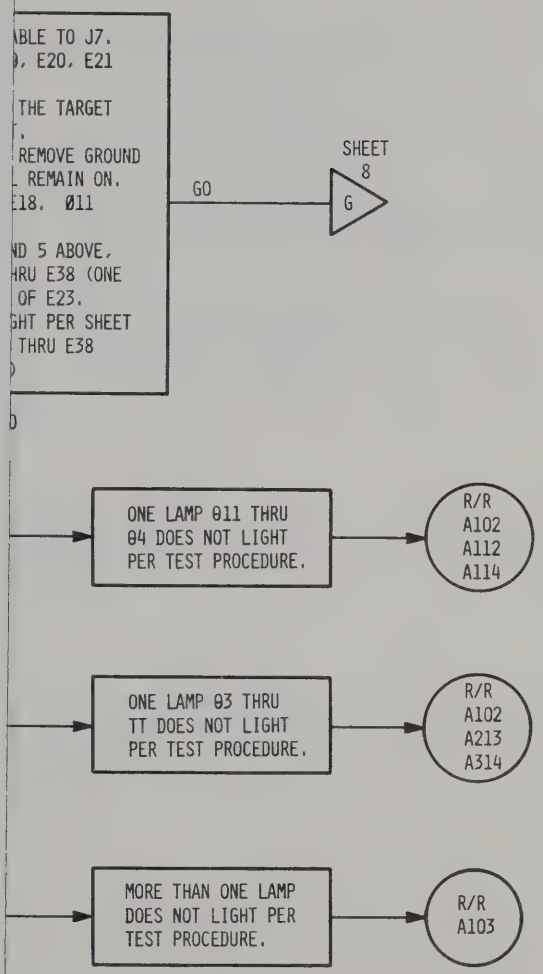

SHEET 4
D
TEST 14
1) SET TARGET SELECTION SWITCHES 2, 8, AND 32 ON.
2) SET SWITCHES 1, 4, 16, 64 AND ALL OFF.
3) APPLY GROUND TO J7-E4 MOMENTARILY.
4) APPLY GROUND TO J7-E5 BETWEEN PULSES AND LEAVE GROUNDED.
5) COUNT THE PULSES UNTIL THE TRACE RISES TO +4V.
6) TRACE SHALL RISE ON PULSE #42. (SEE NOTE 3, PAGE 4).
GO
NO-GO
Q
SHEET 15
TEST 15
1) DISCONNECT CABLES FROM J2 AND J4.
2) SET ALL SWITCH ON.
3) SET GENERATOR FOR A 20 μS PERIOD SQUARE WAVE.
4) SET SCOPE TO 1 MS/DIV.
5) PROBE XA304, PIN 10.
6) MOMENTARILY CONNECT GENERATOR TO J5.
7) VERIFY THAT PULSE BURST APPEARS AS CONNECTION IS MADE.
8) REPEAT TEST ABOVE PROBING XA304, PIN 13, AND XA309 PINS 10, 13, 25, 26, 38, AND 40 ONE AT A TIME.
GO
NO-GO
R/R A304 A309
TEST 16
REPEAT TEST 15 BUT PROBE XA311 P/N 29
GO
NO-GO
R/R A311
TEST 17
1) SET UP 20 μS PERIOD SQUARE WAVE.
2) PROBE XA311, PIN 31.
3) CONNECT GENERATOR TO J7-E5.
4) VERIFY THAT SQUARE WAVE APPEARS ON SCOPE.
5) REPEAT TEST ABOVE WITH GEN. CONNECTED TO E6 THRU E12.
GO
NO-GO
R/R A311
E
SHEET 6

A61036-11-5

FIGURE 5-1. PERFORMANCE TESTS AND FAULT ISOLATION PROCEDURES FLOW DIAGRAM (SHEET 5 OF 17)


MORY
UALLY
E2
RS
GO
SHEET
7
F
R A0 OR A1
NOT GO OUT.
R/R
A207
A2 OR A3
OT GO OUT.
R/R
A206
A4 OR
NOT GO OUT.
R/R
A205
A6 OR A7
OT GO OUT.
R/R
A203
R A8 OR A9
NOT GO OUT.
R/R
A107
R A10 OR AH
NOT GO OUT.
R/R
A106

A61036-11-6



A61036-11-7

ULT ISOLATION PROCEDURES FLOW DIAGRAM (SHEET 7 OF 17)

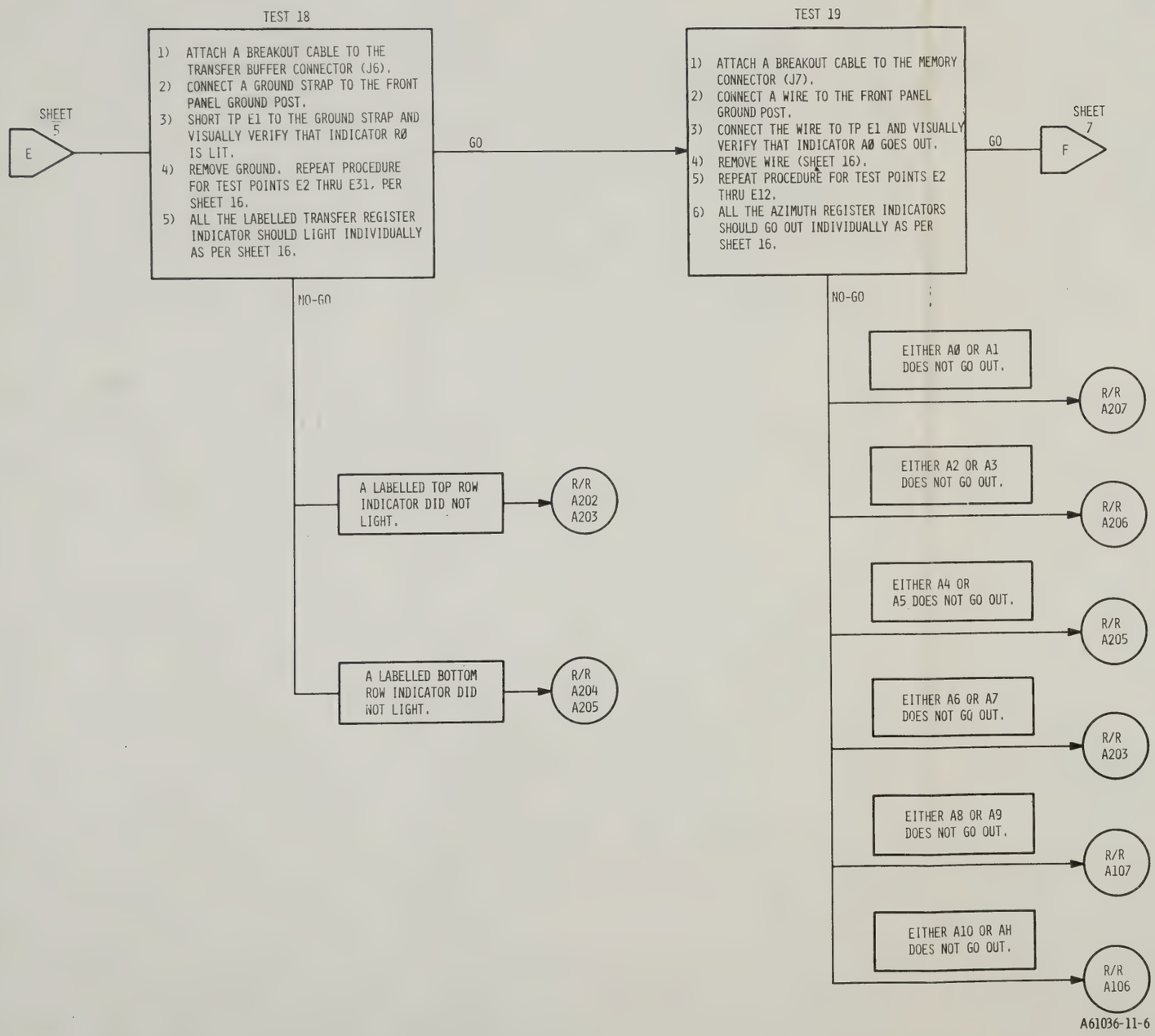
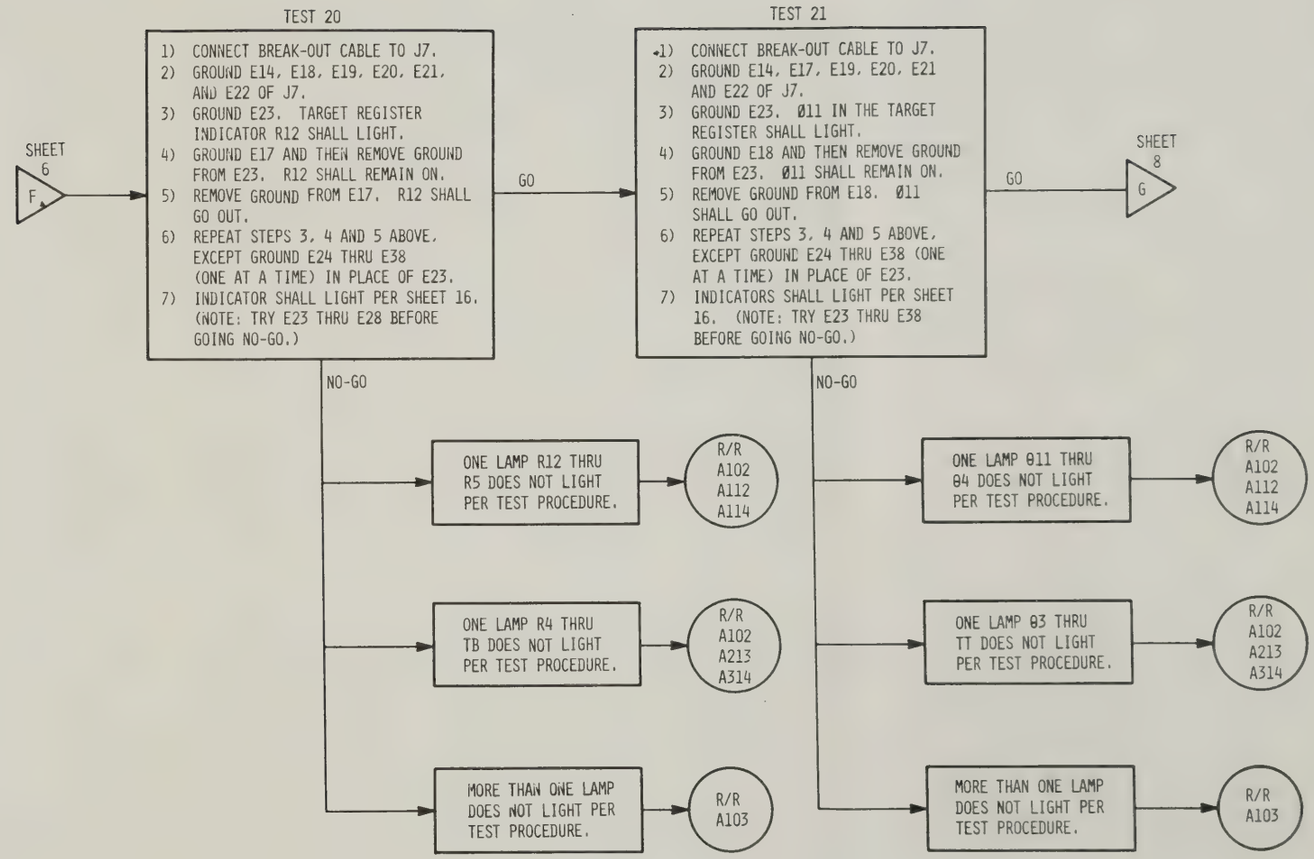

SHEET 5
E
TEST 18
1) ATTACH A BREAKOUT CABLE TO THE TRANSFER BUFFER CONNECTOR (J6).
2) CONNECT A GROUND STRAP TO THE FRONT PANEL GROUND POST.
3) SHORT TP E1 TO THE GROUND STRAP AND VISUALLY VERIFY THAT INDICATOR RØ IS LIT.
4) REMOVE GROUND. REPEAT PROCEDURE FOR TEST POINTS E2 THRU E31, PER SHEET 16.
5) ALL THE LABELLED TRANSFER REGISTER INDICATOR SHOULD LIGHT INDIVIDUALLY AS PER SHEET 16.
GO
NO-GO
A LABELLED TOP ROW INDICATOR DID NOT LIGHT.
R/R A202 A203
A LABELLED BOTTOM ROW INDICATOR DID NOT LIGHT.
R/R A204 A205
TEST 19
1) ATTACH A BREAKOUT CABLE TO THE MEMORY CONNECTOR (J7).
2) CONNECT A WIRE TO THE FRONT PANEL GROUND POST.
3) CONNECT THE WIRE TO TP E1 AND VISUALLY VERIFY THAT INDICATOR AØ GOES OUT.
4) REMOVE WIRE (SHEET 16).
5) REPEAT PROCEDURE FOR TEST POINTS E2 THRU E12.
6) ALL THE AZIMUTH REGISTER INDICATORS SHOULD GO OUT INDIVIDUALLY AS PER SHEET 16.
GO
SHEET 7
F
NO-GO
EITHER AØ OR A1 DOES NOT GO OUT.
R/R A207
EITHER A2 OR A3 DOES NOT GO OUT.
R/R A206
EITHER A4 OR A5 DOES NOT GO OUT.
R/R A205
EITHER A6 OR A7 DOES NOT GO OUT.
R/R A203
EITHER A8 OR A9 DOES NOT GO OUT.
R/R A107
EITHER A10 OR AH DOES NOT GO OUT.
R/R A106
A61036-11-6

FIGURE 5-1. PERFORMANCE TESTS AND FAULT ISOLATION PROCEDURES FLOW DIAGRAM (SHEET 6 OF 17)

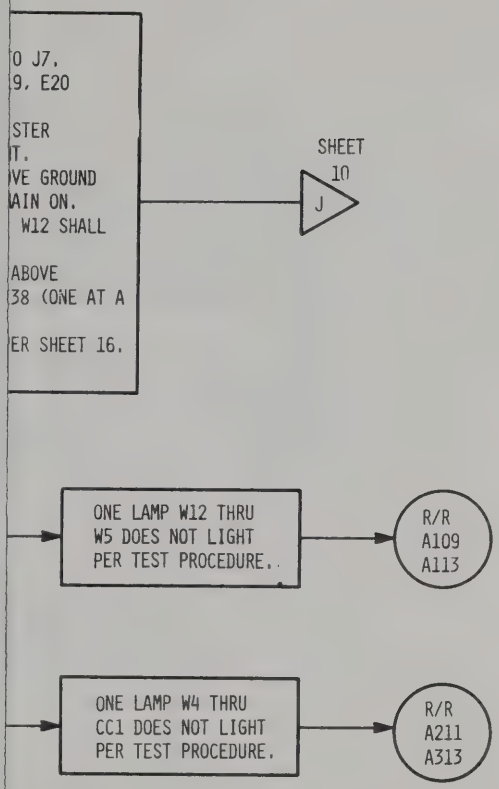

SHEET 6 F
TEST 20
1) CONNECT BREAK-OUT CABLE TO J7.
2) GROUND E14, E18, E19, E20, E21, AND E22 OF J7.
3) GROUND E23. TARGET REGISTER INDICATOR R12 SHALL LIGHT.
4) GROUND E17 AND THEN REMOVE GROUND FROM E23. R12 SHALL REMAIN ON.
5) REMOVE GROUND FROM E17. R12 SHALL GO OUT.
6) REPEAT STEPS 3, 4 AND 5 ABOVE, EXCEPT GROUND E24 THRU E38 (ONE AT A TIME) IN PLACE OF E23.
7) INDICATOR SHALL LIGHT PER SHEET 16. (NOTE: TRY E23 THRU E28 BEFORE GOING NO-GO.)
GO
TEST 21
1) CONNECT BREAK-OUT CABLE TO J7.
2) GROUND E14, E17, E19, E20, E21 AND E22 OF J7.
3) GROUND E23. Ø11 IN THE TARGET REGISTER SHALL LIGHT.
4) GROUND E18 AND THEN REMOVE GROUND FROM E23. Ø11 SHALL REMAIN ON.
5) REMOVE GROUND FROM E18. Ø11 SHALL GO OUT.
6) REPEAT STEPS 3, 4 AND 5 ABOVE, EXCEPT GROUND E24 THRU E38 (ONE AT A TIME) IN PLACE OF E23.
7) INDICATORS SHALL LIGHT PER SHEET 16. (NOTE: TRY E23 THRU E38 BEFORE GOING NO-GO.)
GO
SHEET 8 G
NO-GO
ONE LAMP R12 THRU R5 DOES NOT LIGHT PER TEST PROCEDURE.
R/R A102 A112 A114
ONE LAMP R4 THRU TB DOES NOT LIGHT PER TEST PROCEDURE.
R/R A102 A213 A314
MORE THAN ONE LAMP DOES NOT LIGHT PER TEST PROCEDURE.
R/R A103
NO-GO
ONE LAMP Ø11 THRU Ø4 DOES NOT LIGHT PER TEST PROCEDURE.
R/R A102 A112 A114
ONE LAMP Ø3 THRU TT DOES NOT LIGHT PER TEST PROCEDURE.
R/R A102 A213 A314
MORE THAN ONE LAMP DOES NOT LIGHT PER TEST PROCEDURE.
R/R A103

A61036-11-7

FIGURE 5-1. PERFORMANCE TESTS AND FAULT ISOLATION PROCEDURES FLOW DIAGRAM (SHEET 7 OF 17)

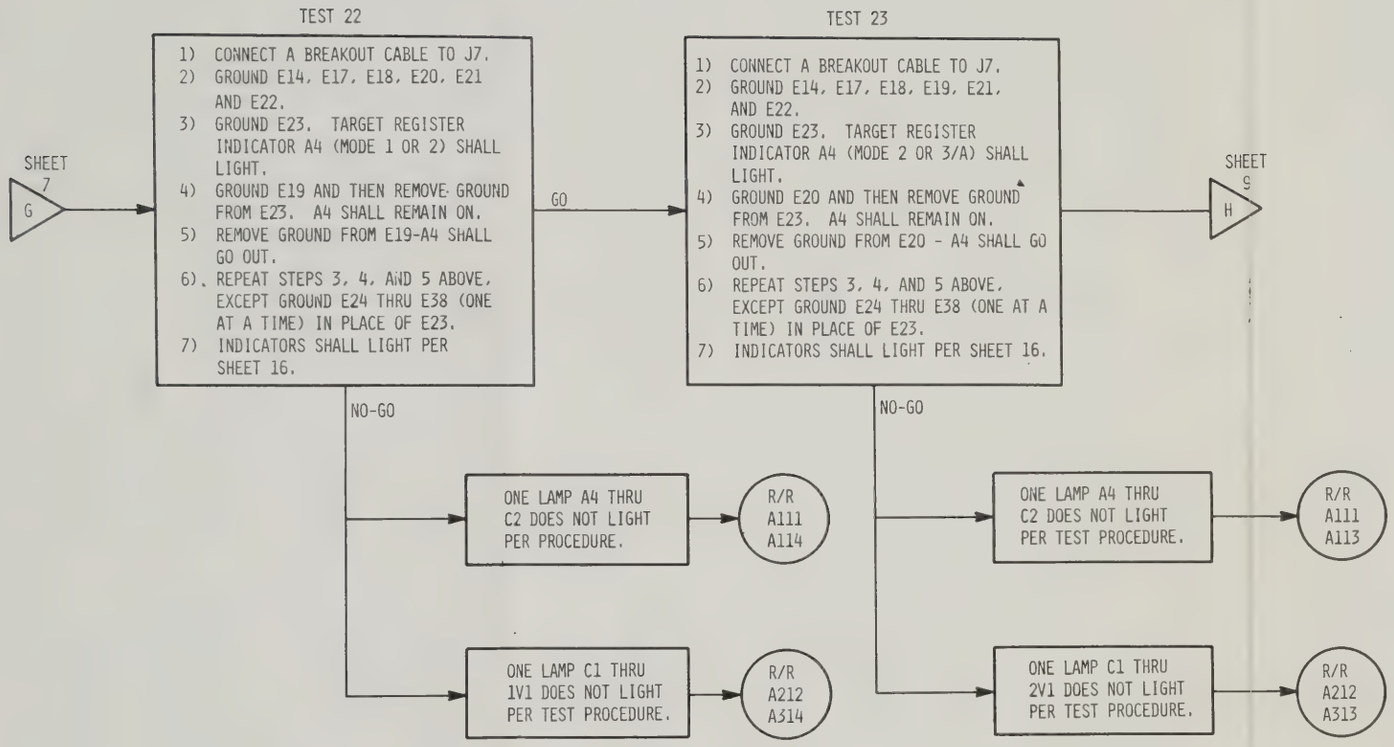
R/R
A111
A113

R/R
A212
A313



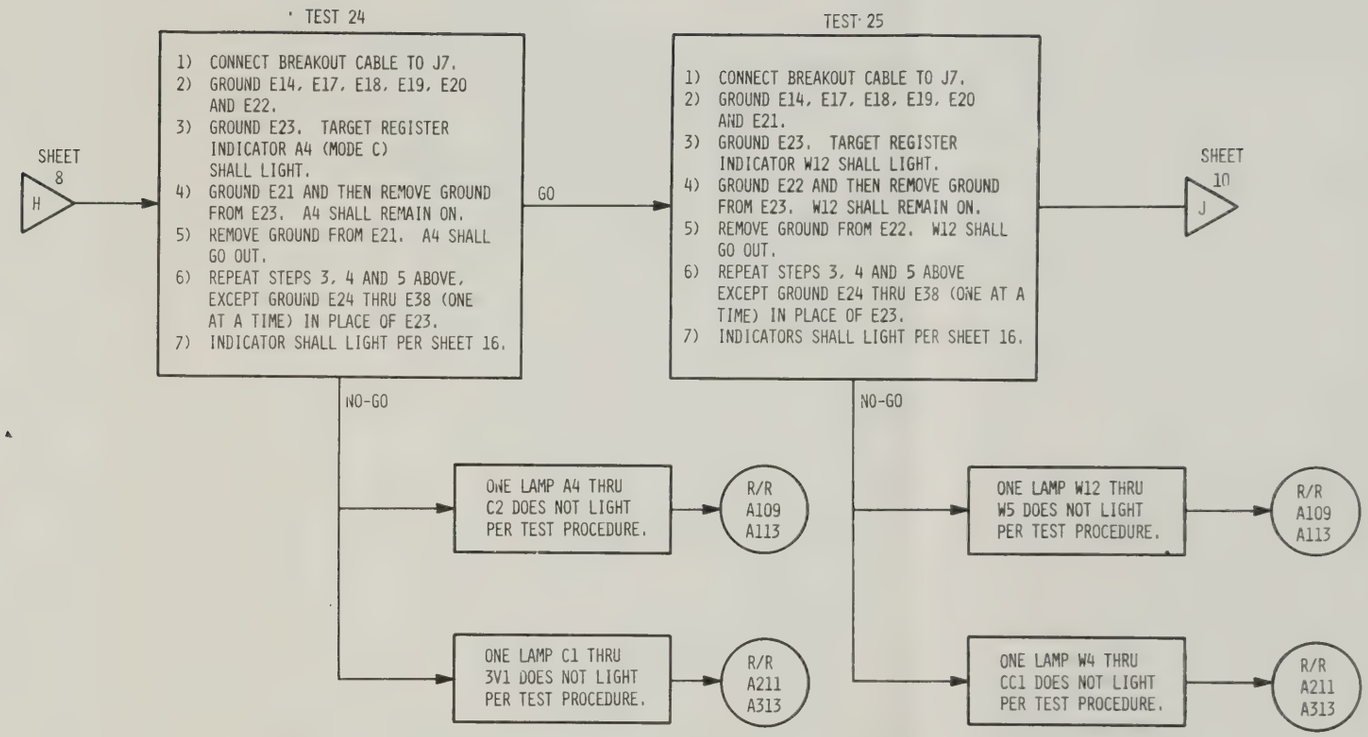
A61036-11-9

SOLATION PROCEDURES FLOW DIAGRAM (SHEET 9 OF 17)


TEST 22
1) CONNECT A BREAKOUT CABLE TO J7.
2) GROUND E14, E17, E18, E20, E21 AND E22.
3) GROUND E23. TARGET REGISTER INDICATOR A4 (MODE 1 OR 2) SHALL LIGHT.
4) GROUND E19 AND THEN REMOVE GROUND FROM E23. A4 SHALL REMAIN ON.
5) REMOVE GROUND FROM E19-A4 SHALL GO OUT.
6) REPEAT STEPS 3, 4, AND 5 ABOVE, EXCEPT GROUND E24 THRU E38 (ONE AT A TIME) IN PLACE OF E23.
7) INDICATORS SHALL LIGHT PER SHEET 16.
SHEET 7 G
GO
TEST 23
1) CONNECT A BREAKOUT CABLE TO J7.
2) GROUND E14, E17, E18, E19, E21, AND E22.
3) GROUND E23. TARGET REGISTER INDICATOR A4 (MODE 2 OR 3/A) SHALL LIGHT.
4) GROUND E20 AND THEN REMOVE GROUND FROM E23. A4 SHALL REMAIN ON.
5) REMOVE GROUND FROM E20 - A4 SHALL GO OUT.
6) REPEAT STEPS 3, 4, AND 5 ABOVE, EXCEPT GROUND E24 THRU E38 (ONE AT A TIME) IN PLACE OF E23.
7) INDICATORS SHALL LIGHT PER SHEET 16.
SHEET 9 H
NO-GO
ONE LAMP A4 THRU C2 DOES NOT LIGHT PER PROCEDURE.
R/R A111 A114
ONE LAMP C1 THRU 1V1 DOES NOT LIGHT PER TEST PROCEDURE.
R/R A212 A314
NO-GO
ONE LAMP A4 THRU C2 DOES NOT LIGHT PER TEST PROCEDURE.
R/R A111 A113
ONE LAMP C1 THRU 2V1 DOES NOT LIGHT PER TEST PROCEDURE.
R/R A212 A313

A61036-11-8

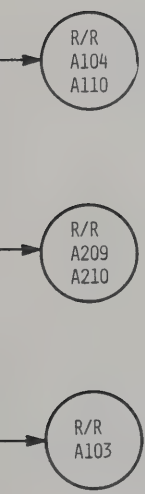
FIGURE 5-1. PERFORMANCE TESTS AND FAULT ISOLATION PROCEDURES FLOW DIAGRAM (SHEET 8 OF 17)

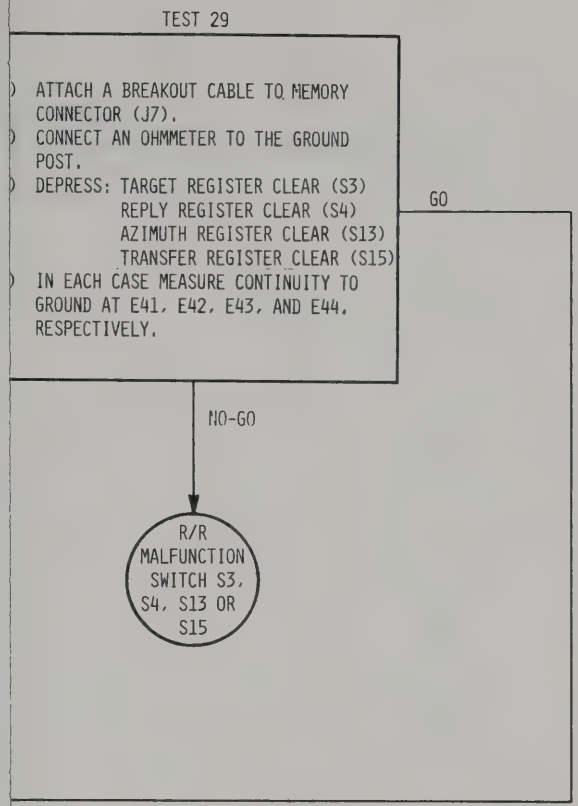

SHEET 8
H
TEST 24
1) CONNECT BREAKOUT CABLE TO J7.
2) GROUND E14, E17, E18, E19, E20 AND E22.
3) GROUND E23. TARGET REGISTER INDICATOR A4 (MODE C) SHALL LIGHT.
4) GROUND E21 AND THEN REMOVE GROUND FROM E23. A4 SHALL REMAIN ON.
5) REMOVE GROUND FROM E21. A4 SHALL GO OUT.
6) REPEAT STEPS 3, 4 AND 5 ABOVE, EXCEPT GROUND E24 THRU E38 (ONE AT A TIME) IN PLACE OF E23.
7) INDICATOR SHALL LIGHT PER SHEET 16.
GO
TEST 25
1) CONNECT BREAKOUT CABLE TO J7.
2) GROUND E14, E17, E18, E19, E20 AND E21.
3) GROUND E23. TARGET REGISTER INDICATOR W12 SHALL LIGHT.
4) GROUND E22 AND THEN REMOVE GROUND FROM E23. W12 SHALL REMAIN ON.
5) REMOVE GROUND FROM E22. W12 SHALL GO OUT.
6) REPEAT STEPS 3, 4 AND 5 ABOVE EXCEPT GROUND E24 THRU E38 (ONE AT A TIME) IN PLACE OF E23.
7) INDICATORS SHALL LIGHT PER SHEET 16.
SHEET 10
J
NO-GO
NO-GO
ONE LAMP A4 THRU C2 DOES NOT LIGHT PER TEST PROCEDURE.
R/R A109 A113
ONE LAMP W12 THRU W5 DOES NOT LIGHT PER TEST PROCEDURE.
R/R A109 A113
ONE LAMP C1 THRU 3V1 DOES NOT LIGHT PER TEST PROCEDURE.
R/R A211 A313
ONE LAMP W4 THRU CC1 DOES NOT LIGHT PER TEST PROCEDURE.
R/R A211 A313

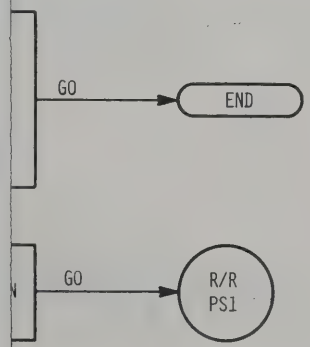
A61036-11-9

FIGURE 5-1. PERFORMANCE TESTS AND FAULT ISOLATION PROCEDURES FLOW DIAGRAM (SHEET 9 OF 17)

SHEET 11

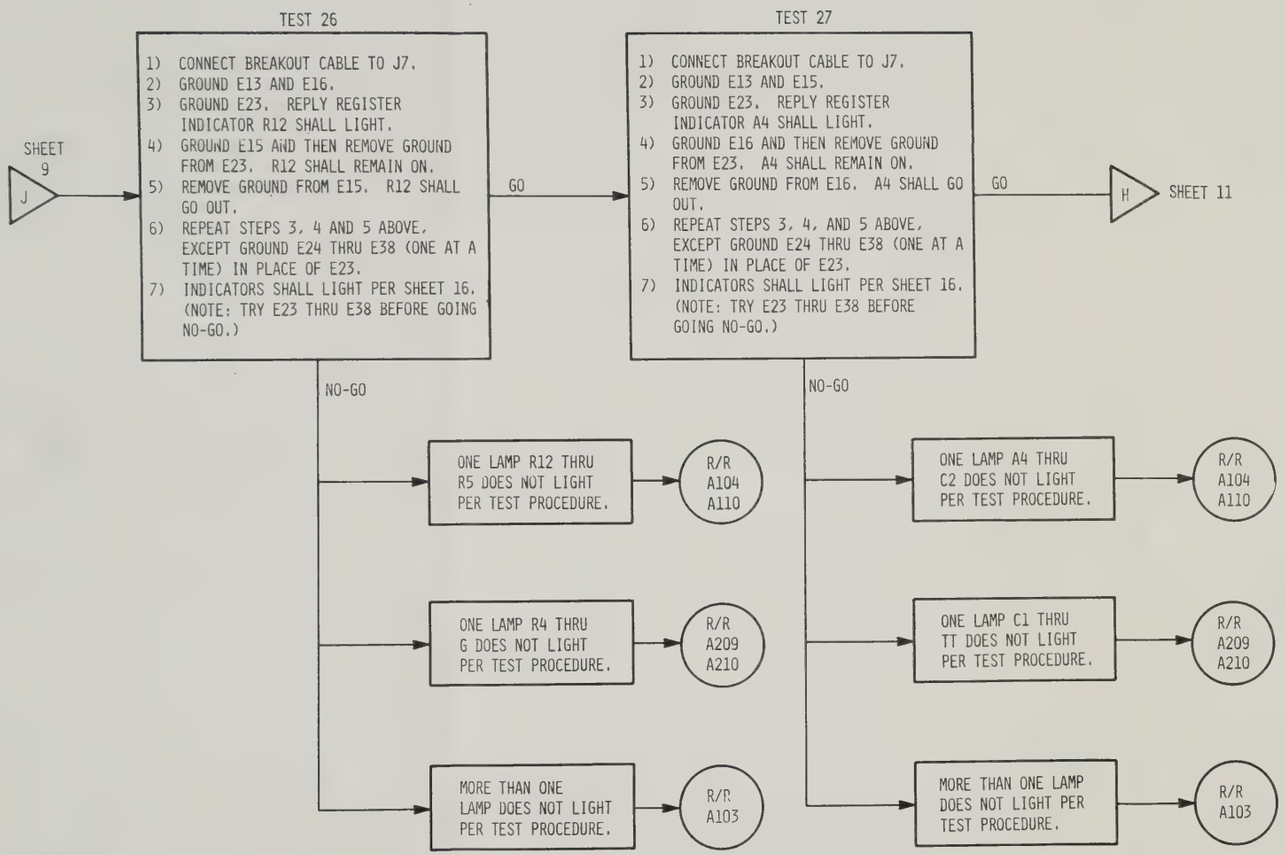



TEST 29
ATTACH A BREAKOUT CABLE TO MEMORY CONNECTOR (J7).
CONNECT AN OHMMETER TO THE GROUND POST.
DEPRESS: TARGET REGISTER CLEAR (S3)
REPLY REGISTER CLEAR (S4)
AZIMUTH REGISTER CLEAR (S13)
TRANSFER REGISTER CLEAR (S15)
IN EACH CASE MEASURE CONTINUITY TO GROUND AT E41, E42, E43, AND E44, RESPECTIVELY.
GO
NO-GO
R/R MALFUNCTION SWITCH S3, S4, S13 OR S15



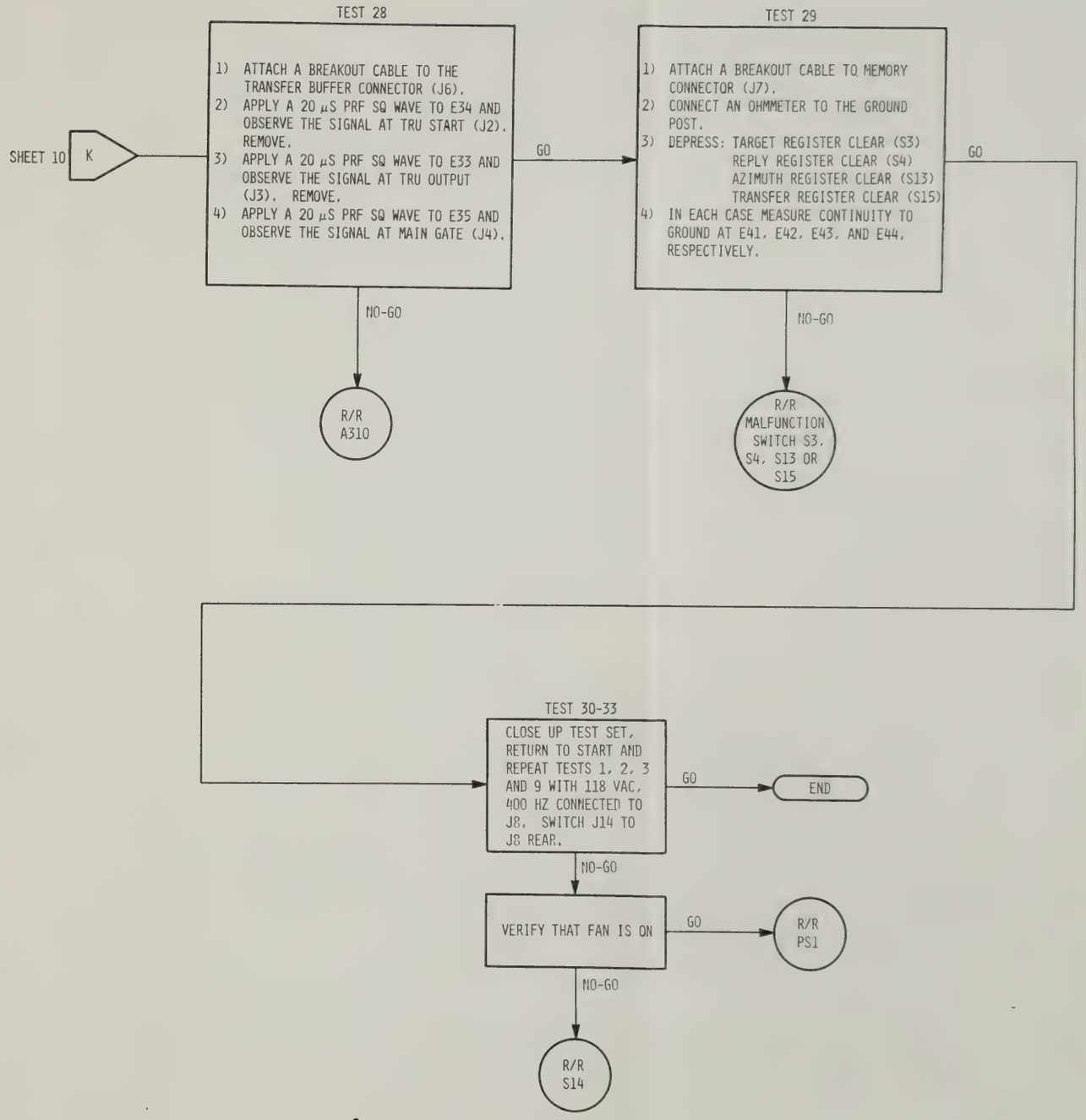
A61036-11-11

FAULT ISOLATION PROCEDURES FLOW DIAGRAM (SHEET 11 OF 17)


TEST 26
1) CONNECT BREAKOUT CABLE TO J7.
2) GROUND E13 AND E16.
3) GROUND E23. REPLY REGISTER INDICATOR R12 SHALL LIGHT.
4) GROUND E15 AND THEN REMOVE GROUND FROM E23. R12 SHALL REMAIN ON.
5) REMOVE GROUND FROM E15. R12 SHALL GO OUT.
6) REPEAT STEPS 3, 4 AND 5 ABOVE, EXCEPT GROUND E24 THRU E38 (ONE AT A TIME) IN PLACE OF E23.
7) INDICATORS SHALL LIGHT PER SHEET 16. (NOTE: TRY E23 THRU E38 BEFORE GOING NO-GO.)
SHEET 9
J
GO
TEST 27
1) CONNECT BREAKOUT CABLE TO J7.
2) GROUND E13 AND E15.
3) GROUND E23. REPLY REGISTER INDICATOR A4 SHALL LIGHT.
4) GROUND E16 AND THEN REMOVE GROUND FROM E23. A4 SHALL REMAIN ON.
5) REMOVE GROUND FROM E16. A4 SHALL GO OUT.
6) REPEAT STEPS 3, 4, AND 5 ABOVE, EXCEPT GROUND E24 THRU E38 (ONE AT A TIME) IN PLACE OF E23.
7) INDICATORS SHALL LIGHT PER SHEET 16. (NOTE: TRY E23 THRU E38 BEFORE GOING NO-GO.)
GO
H
SHEET 11
NO-GO
NO-GO
ONE LAMP R12 THRU R5 DOES NOT LIGHT PER TEST PROCEDURE.
R/R A104 A110
ONE LAMP R4 THRU G DOES NOT LIGHT PER TEST PROCEDURE.
R/R A209 A210
MORE THAN ONE LAMP DOES NOT LIGHT PER TEST PROCEDURE.
R/R A103
ONE LAMP A4 THRU C2 DOES NOT LIGHT PER TEST PROCEDURE.
R/R A104 A110
ONE LAMP C1 THRU TT DOES NOT LIGHT PER TEST PROCEDURE.
R/R A209 A210
MORE THAN ONE LAMP DOES NOT LIGHT PER TEST PROCEDURE.
R/R A103

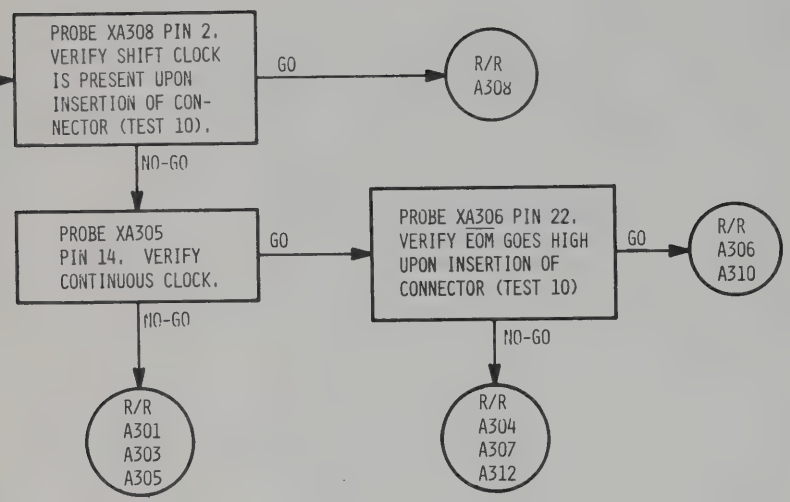
A61036-11-10

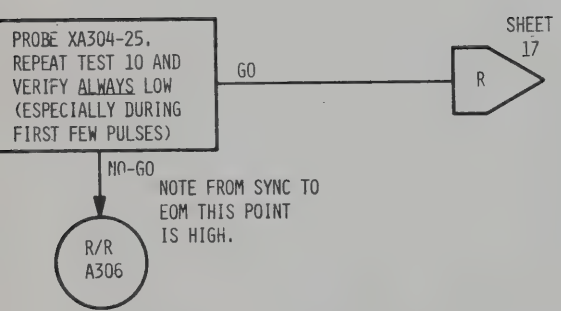
FIGURE 5-1. PERFORMANCE TESTS AND FAULT ISOLATION PROCEDURES FLOW DIAGRAM (SHEET 10 OF 17)


TEST 28
1) ATTACH A BREAKOUT CABLE TO THE TRANSFER BUFFER CONNECTOR (J6).
2) APPLY A 20 μS PRF SQ WAVE TO E34 AND OBSERVE THE SIGNAL AT TRU START (J2). REMOVE.
3) APPLY A 20 μS PRF SQ WAVE TO E33 AND OBSERVE THE SIGNAL AT TRU OUTPUT (J3). REMOVE.
4) APPLY A 20 μS PRF SQ WAVE TO E35 AND OBSERVE THE SIGNAL AT MAIN GATE (J4).
SHEET 10 K
GO
NO-GO
R/R A310
TEST 29
1) ATTACH A BREAKOUT CABLE TO MEMORY CONNECTOR (J7).
2) CONNECT AN OHMMETER TO THE GROUND POST.
3) DEPRESS: TARGET REGISTER CLEAR (S3)
REPLY REGISTER CLEAR (S4)
AZIMUTH REGISTER CLEAR (S13)
TRANSFER REGISTER CLEAR (S15)
4) IN EACH CASE MEASURE CONTINUITY TO GROUND AT E41, E42, E43, AND E44, RESPECTIVELY.
GO
NO-GO
R/R MALFUNCTION SWITCH S3, S4, S13 OR S15
TEST 30-33
CLOSE UP TEST SET, RETURN TO START AND REPEAT TESTS 1, 2, 3 AND 9 WITH 118 VAC, 400 HZ CONNECTED TO J8. SWITCH J14 TO J8 REAR.
GO
END
NO-GO
VERIFY THAT FAN IS ON
GO
R/R PS1
NO-GO
R/R S14

A61036-11-11

FIGURE 5-1. PERFORMANCE TESTS AND FAULT ISOLATION PROCEDURES FLOW DIAGRAM (SHEET 11 OF 17)


PROBE XA308 PIN 2. VERIFY SHIFT CLOCK IS PRESENT UPON INSERTION OF CONNECTOR (TEST 10).
GO
R/R A308
NO-GO
PROBE XA305 PIN 14. VERIFY CONTINUOUS CLOCK.
GO
PROBE XA306 PIN 22. VERIFY EOM GOES HIGH UPON INSERTION OF CONNECTOR (TEST 10)
GO
R/R A306 A310
NO-GO
NO-GO
R/R A301 A303 A305
R/R A304 A307 A312


PROBE XA304-25. REPEAT TEST 10 AND VERIFY ALWAYS LOW (ESPECIALLY DURING FIRST FEW PULSES)
GO
SHEET 17
R
NO-GO
NOTE FROM SYNC TO EOM THIS POINT IS HIGH.
R/R A306

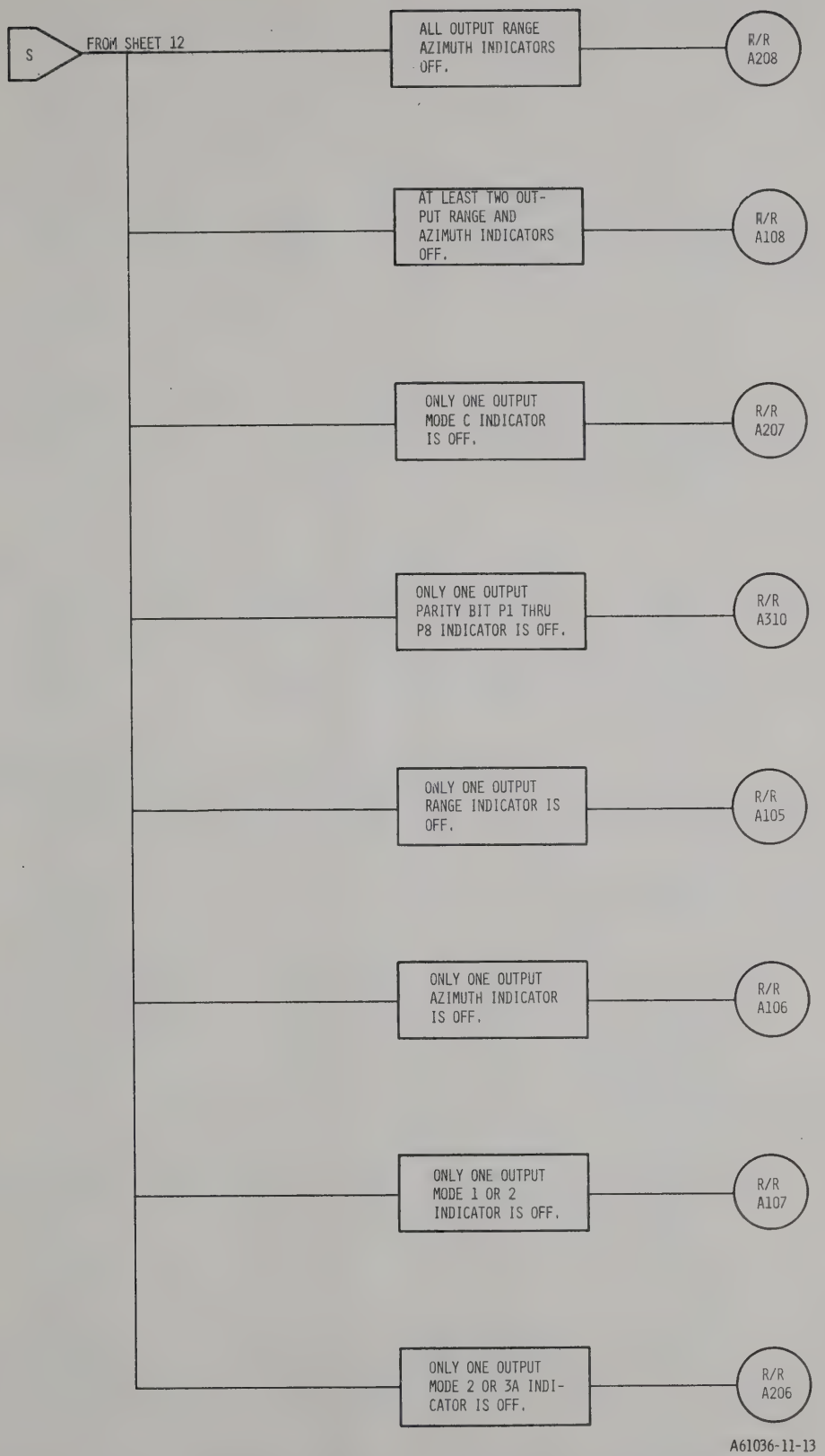
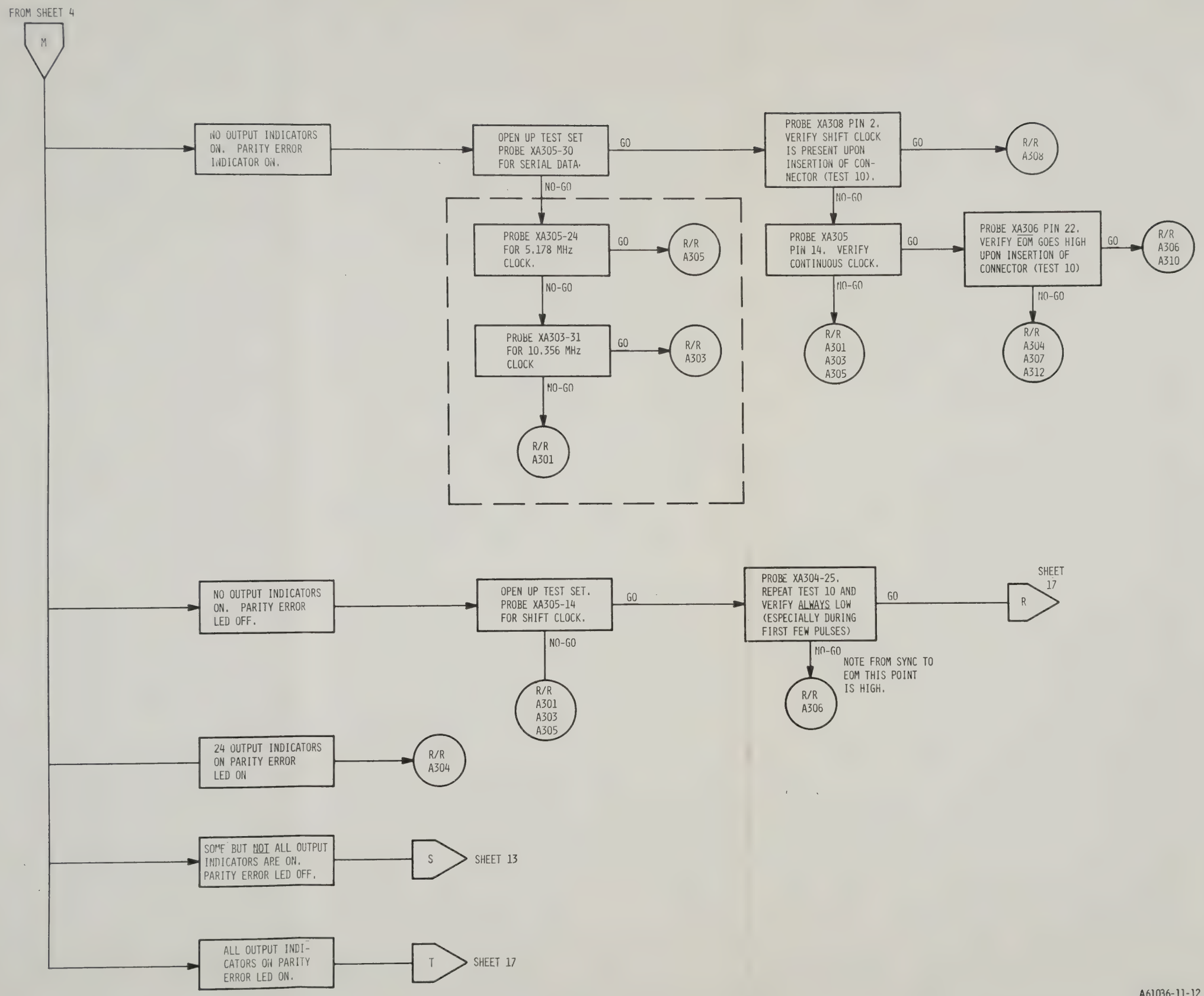

S
FROM SHEET 12
ALL OUTPUT RANGE AZIMUTH INDICATORS OFF.
R/R A208
AT LEAST TWO OUTPUT RANGE AND AZIMUTH INDICATORS OFF.
R/R A108
ONLY ONE OUTPUT MODE C INDICATOR IS OFF.
R/R A207
ONLY ONE OUTPUT PARITY BIT P1 THRU P8 INDICATOR IS OFF.
R/R A310
ONLY ONE OUTPUT RANGE INDICATOR IS OFF.
R/R A105
ONLY ONE OUTPUT AZIMUTH INDICATOR IS OFF.
R/R A106
ONLY ONE OUTPUT MODE 1 OR 2 INDICATOR IS OFF.
R/R A107
ONLY ONE OUTPUT MODE 2 OR 3A INDICATOR IS OFF.
R/R A206
A61036-11-13

FIGURE 5-1. PERFORMANCE TESTS AND FAULT ISOLATION PROCEDURES FLOW DIAGRAM (SHEET 13 OF 17)



A61036-11-12

FIGURE 5-1. PERFORMANCE TESTS AND FAULT ISOLATION PROCEDURES FLOW DIAGRAM (SHEET 12 OF 17)

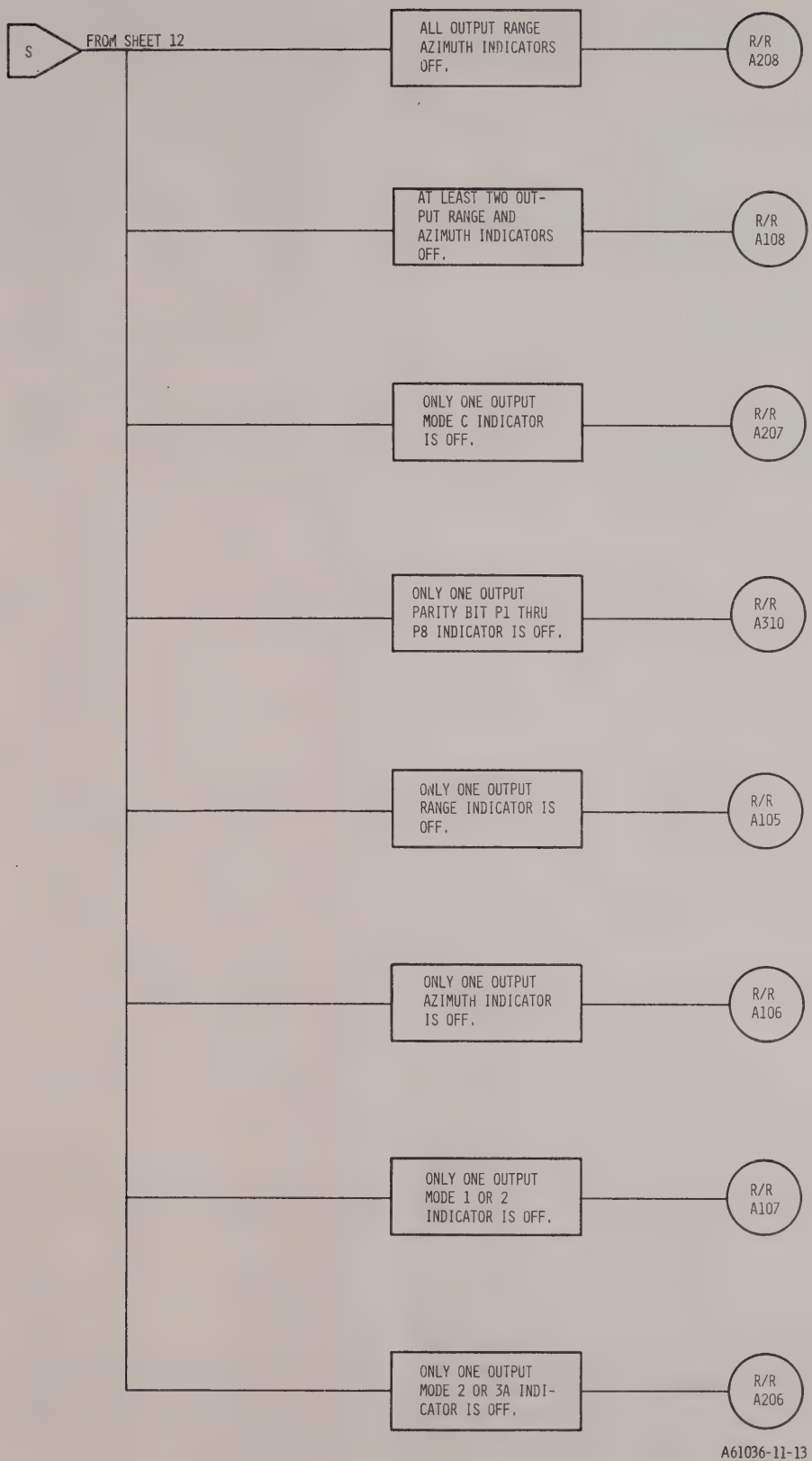

S
FROM SHEET 12
ALL OUTPUT RANGE AZIMUTH INDICATORS OFF.
R/R A208
AT LEAST TWO OUTPUT RANGE AND AZIMUTH INDICATORS OFF.
R/R A108
ONLY ONE OUTPUT MODE C INDICATOR IS OFF.
R/R A207
ONLY ONE OUTPUT PARITY BIT P1 THRU P8 INDICATOR IS OFF.
R/R A310
ONLY ONE OUTPUT RANGE INDICATOR IS OFF.
R/R A105
ONLY ONE OUTPUT AZIMUTH INDICATOR IS OFF.
R/R A106
ONLY ONE OUTPUT MODE 1 OR 2 INDICATOR IS OFF.
R/R A107
ONLY ONE OUTPUT MODE 2 OR 3A INDICATOR IS OFF.
R/R A206
A61036-11-13

FIGURE 5-1. PERFORMANCE TESTS AND FAULT ISOLATION PROCEDURES FLOW DIAGRAM (SHEET 13 OF 17)

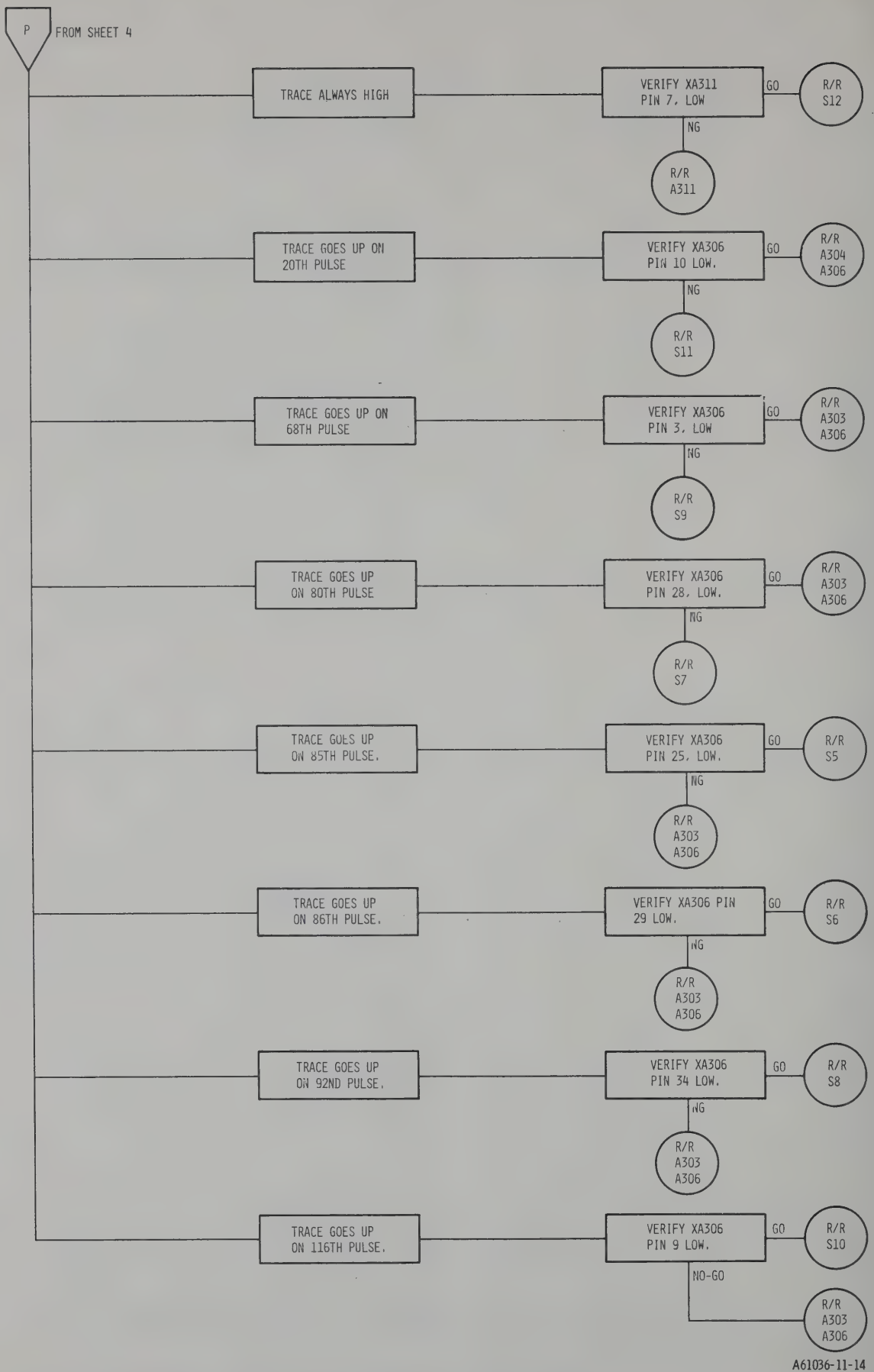
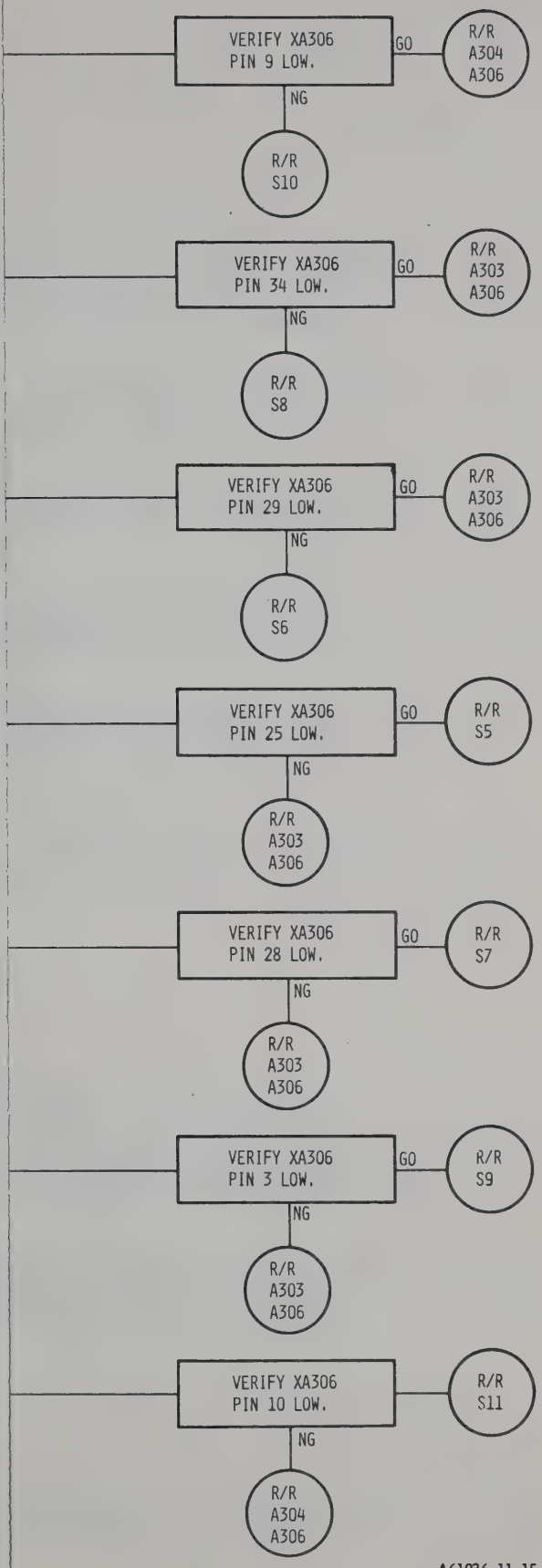


FIGURE 5-1. PERFORMANCE TESTS AND FAULT ISOLATION PROCEDURES FLOW DIAGRAM (SHEET 14 OF 17)



A61036-11-15

D FAULT ISOLATION PROCEDURES FLOW DIAGRAM (SHEET 15 OF 17)

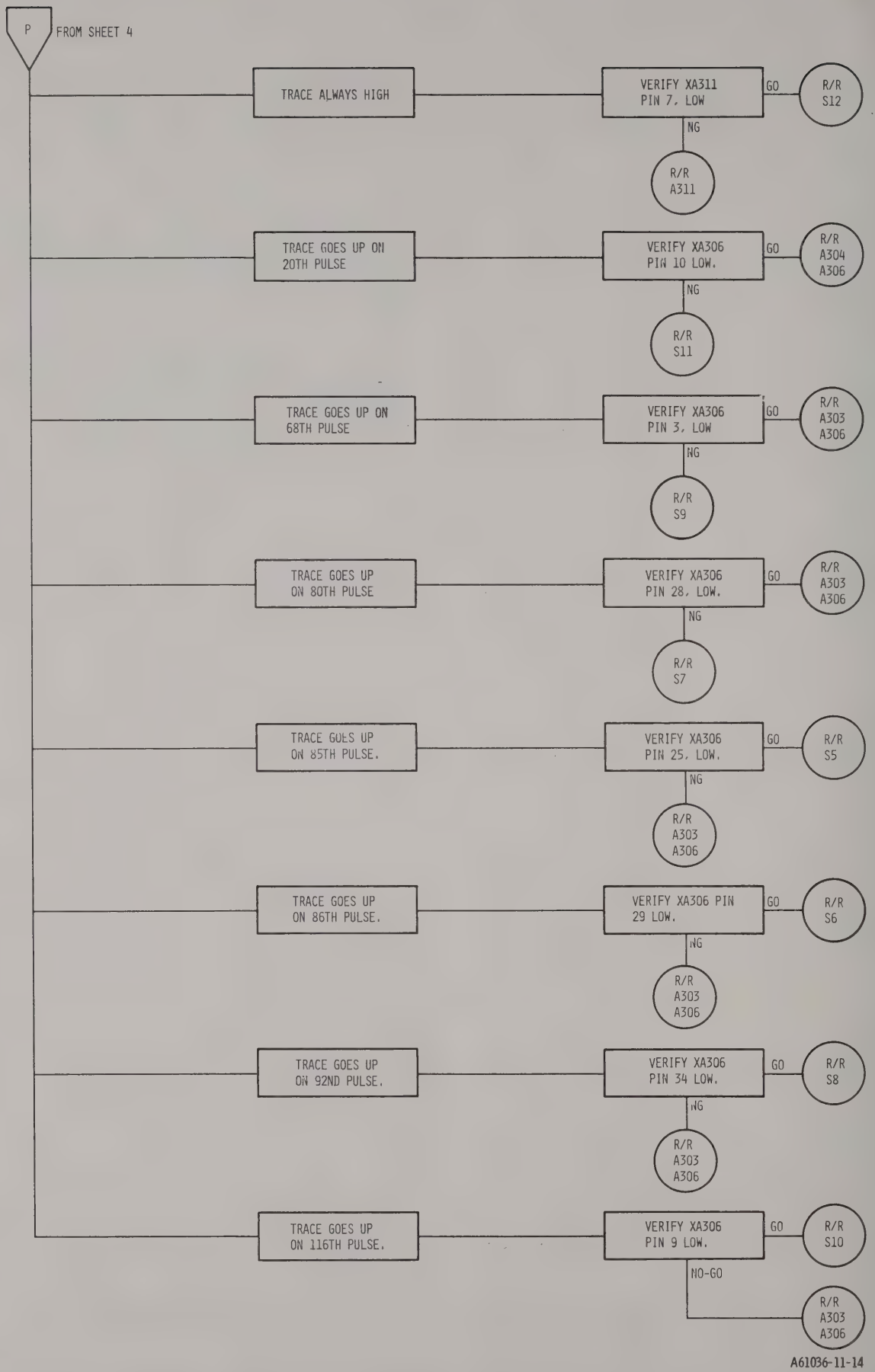
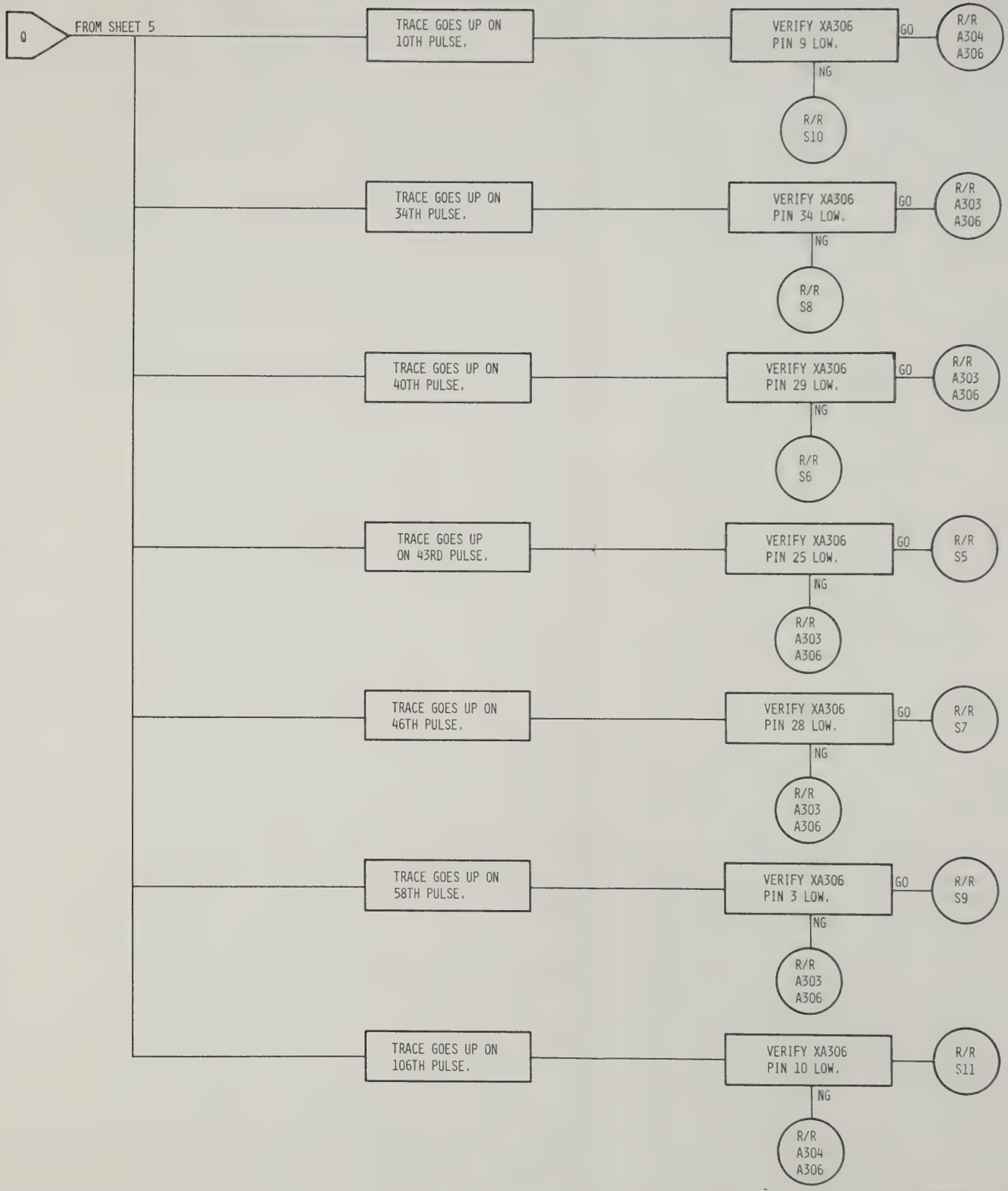
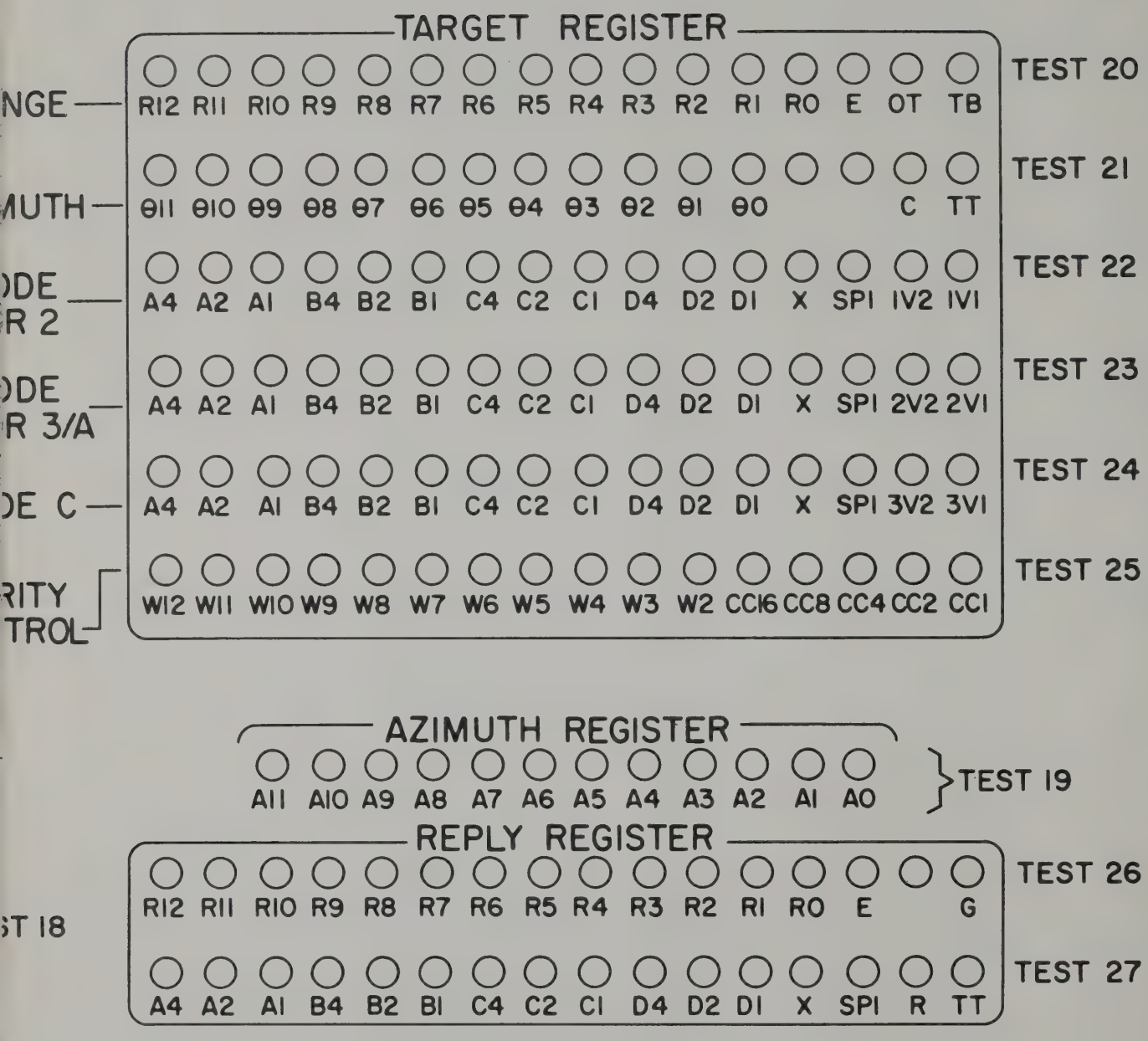


FIGURE 5-1. PERFORMANCE TESTS AND FAULT ISOLATION PROCEDURES FLOW DIAGRAM (SHEET 14 OF 17)



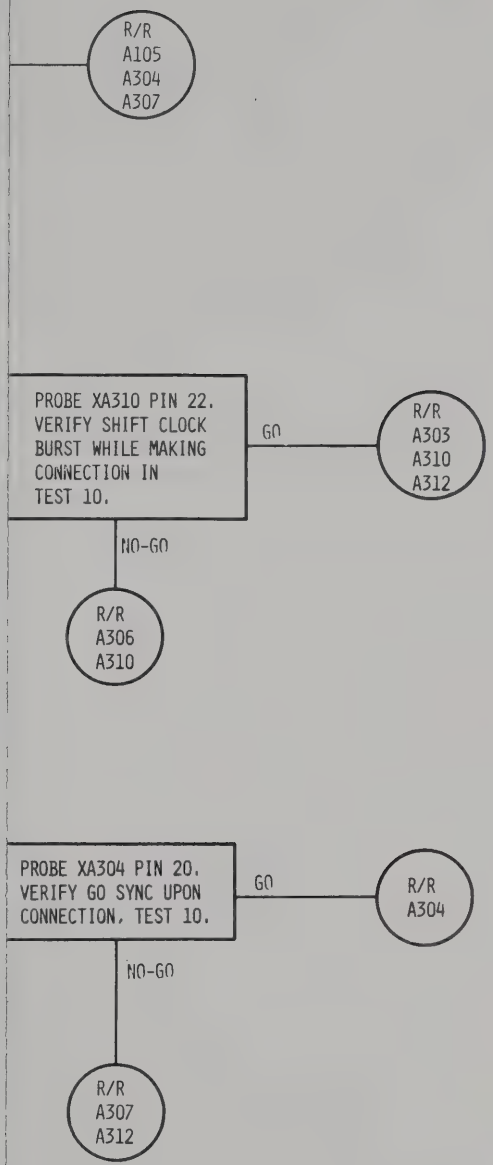
A61036-11-15

FIGURE 5-1. PERFORMANCE TESTS AND FAULT ISOLATION PROCEDURES FLOW DIAGRAM (SHEET 15 OF 17)


TARGET REGISTER
R12 R11 R10 R9 R8 R7 R6 R5 R4 R3 R2 R1 R0 E OT TB
TEST 20
θ11 θ10 θ9 θ8 θ7 θ6 θ5 θ4 θ3 θ2 θ1 θ0 C TT
TEST 21
A4 A2 A1 B4 B2 B1 C4 C2 C1 D4 D2 D1 X SPI IV2 IV1
TEST 22
A4 A2 A1 B4 B2 B1 C4 C2 C1 D4 D2 D1 X SPI 2V2 2V1
TEST 23
A4 A2 A1 B4 B2 B1 C4 C2 C1 D4 D2 D1 X SPI 3V2 3V1
TEST 24
W12 W11 W10 W9 W8 W7 W6 W5 W4 W3 W2 CC16 CC8 CC4 CC2 CC1
TEST 25
AZIMUTH REGISTER
A11 A10 A9 A8 A7 A6 A5 A4 A3 A2 A1 A0
TEST 19
REPLY REGISTER
R12 R11 R10 R9 R8 R7 R6 R5 R4 R3 R2 R1 R0 E G
TEST 26
A4 A2 A1 B4 B2 B1 C4 C2 C1 D4 D2 D1 X SPI R TT
TEST 27

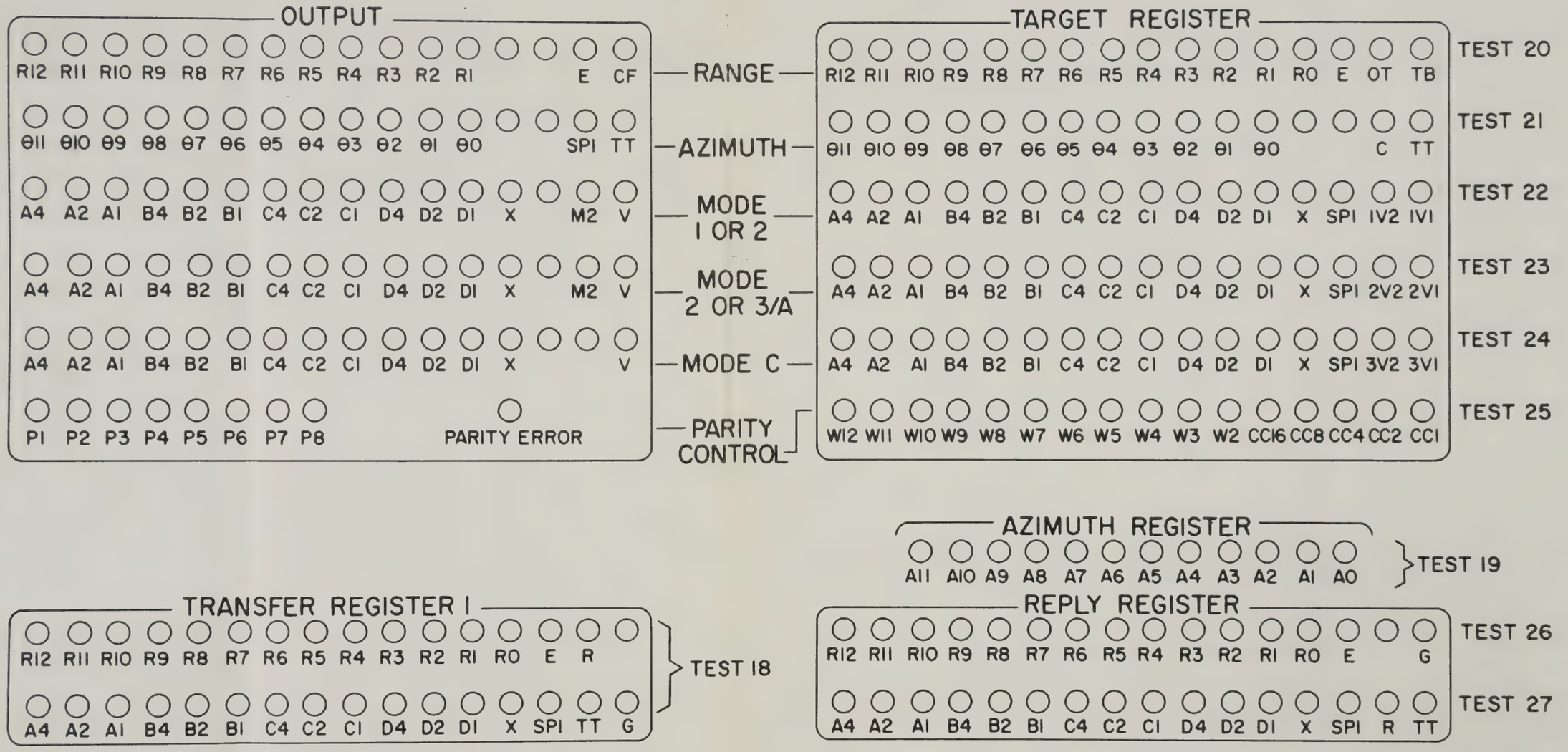
A61036-11-16

OW DIAGRAM (SHEET 16 OF 17)



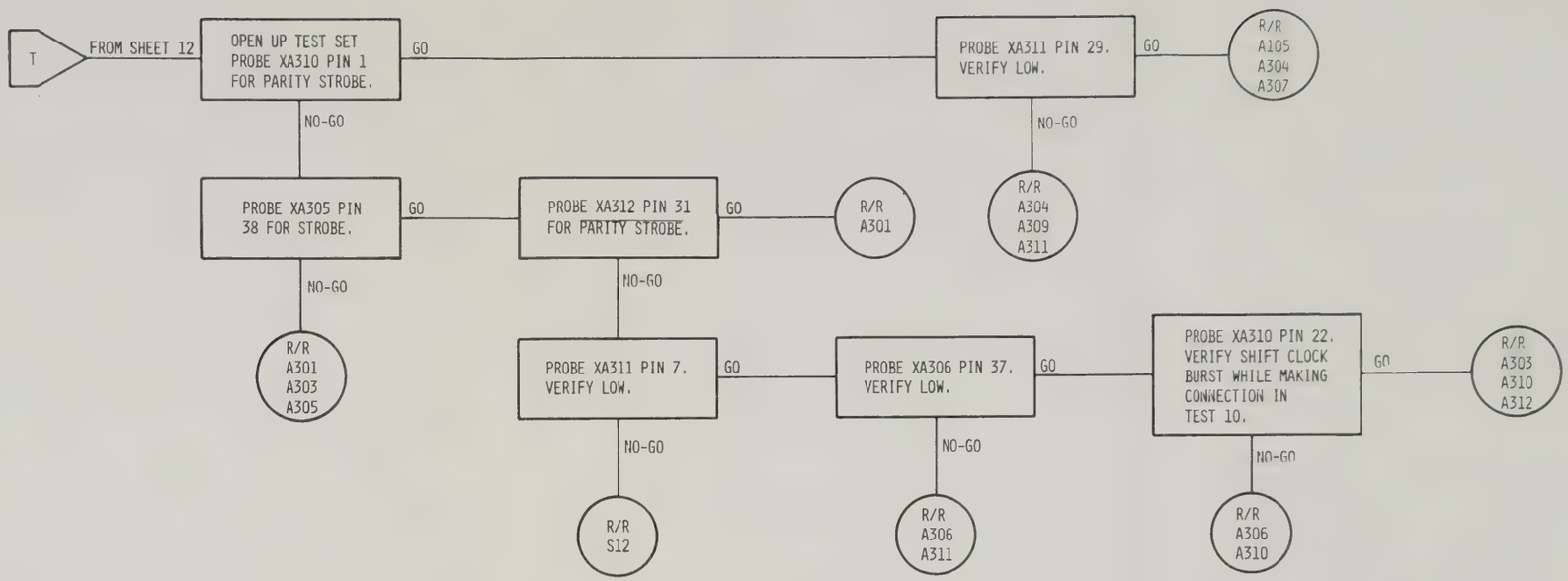
A61036-11-17

OLATION PROCEDURES FLOW DIAGRAM (SHEET 17 OF 17)


OUTPUT
R12 R11 R10 R9 R8 R7 R6 R5 R4 R3 R2 R1 E CF
θ11 θ10 θ9 θ8 θ7 θ6 θ5 θ4 θ3 θ2 θ1 θ0 SPI TT
A4 A2 A1 B4 B2 B1 C4 C2 C1 D4 D2 D1 X M2 V
A4 A2 A1 B4 B2 B1 C4 C2 C1 D4 D2 D1 X M2 V
A4 A2 A1 B4 B2 B1 C4 C2 C1 D4 D2 D1 X V
P1 P2 P3 P4 P5 P6 P7 P8 PARITY ERROR
RANGE
AZIMUTH
MODE 1 OR 2
MODE 2 OR 3/A
MODE C
PARITY CONTROL
TARGET REGISTER
R12 R11 R10 R9 R8 R7 R6 R5 R4 R3 R2 R1 R0 E OT TB
θ11 θ10 θ9 θ8 θ7 θ6 θ5 θ4 θ3 θ2 θ1 θ0 C TT
A4 A2 A1 B4 B2 B1 C4 C2 C1 D4 D2 D1 X SPI IV2 IV1
A4 A2 A1 B4 B2 B1 C4 C2 C1 D4 D2 D1 X SPI 2V2 2V1
A4 A2 A1 B4 B2 B1 C4 C2 C1 D4 D2 D1 X SPI 3V2 3V1
W12 W11 W10 W9 W8 W7 W6 W5 W4 W3 W2 CC16 CC8 CC4 CC2 CC1
TEST 20
TEST 21
TEST 22
TEST 23
TEST 24
TEST 25
AZIMUTH REGISTER
A11 A10 A9 A8 A7 A6 A5 A4 A3 A2 A1 A0
TEST 19
TRANSFER REGISTER I
R12 R11 R10 R9 R8 R7 R6 R5 R4 R3 R2 R1 R0 E R
A4 A2 A1 B4 B2 B1 C4 C2 C1 D4 D2 D1 X SPI TT G
TEST 18
REPLY REGISTER
R12 R11 R10 R9 R8 R7 R6 R5 R4 R3 R2 R1 R0 E G
A4 A2 A1 B4 B2 B1 C4 C2 C1 D4 D2 D1 X SPI R TT
TEST 26
TEST 27

A61036-11-16

FIGURE 5-1. PERFORMANCE TESTS AND FAULT ISOLATION PROCEDURES FLOW DIAGRAM (SHEET 16 OF 17)



A61036-11-17

FIGURE 5-1. PERFORMANCE TESTS AND FAULT ISOLATION PROCEDURES FLOW DIAGRAM (SHEET 17 OF 17)

5-17. The diagnostics assume the following basic rules:

a. Only one failure at a time has occurred. (Chain reactions possible in a given failure mode are considered by the diagnostic.)

b. Failures are of a random nature and not due to accidental physical damage. (Normally, such faults can be discovered by visual inspection; if not, use the diagnostics.)

c. Internal wiring and interconnections are assumed good.

5-18. ERRORS MADE IN FAULT ISOLATING. If, during fault isolation, the specified corrective action fails to correct the observed symptom, perform the following steps:

a. Check the interconnections to the suspected circuit card or component.

b. If possible, as with a printed circuit board, check the suspected component. More than one malfunction may have occurred at different times and gone uncorrected. If the component has malfunctioned, repeat the diagnostic process until the other malfunction is discovered. Correct each malfunction as it is discovered.

c. If steps a. or b. do not correct the fault, carefully retrace the diagnostic steps making certain that all parameters of a specified indication are evaluated.

5-19. DC VOLTAGE REQUIREMENTS AND SOURCES.

5-20. The DC voltage requirements and sources are included in figure 5-1 performance tests and fault isolation procedures.

5-21. ALIGNMENT AND ADJUSTMENT PROCEDURES.

5-22. There are no electrical alignment instructions required for the components of this test set. For power supply adjustments refer to T.O. 33D7-6-24-2.

5-23. A mechanical alignment of the test set front panel with the interfacing electronic assembly is required whenever the front panel is removed from the electronic assembly for part replacement.

NOTE

If the front panel is not properly aligned with the electronic assembly, it may be difficult to install the electronic assembly in the combination case.

5-24. To ensure that the front panel is properly aligned or connected to the electronic assembly during reassembly, proceed as follows:

a. When connecting the front panel to the electronic assembly, the front panel screws should be loosely secured.

b. Slide the electronic assembly into the combination case along the internal guide rails until the rear alignment pins are engaged.

c. With the front panel slightly secured, adjust the front panel until the assembly can be fully seated into the combination case.

d. Tighten the front panel securing screws.

SECTION II

SPECIAL MAINTENANCE

5-25. Special maintenance instructions for the test set are applicable for circuit cards and power supply subassemblies only. For special maintenance instructions for circuit cards refer to Chapter 3 of the Electronics Plug-In Unit Test Set AN/TPM-36 (T.O. 33D7-49-55-2). For special maintenance instructions for power supplies refer to Chapter 3 of the Power Supply Test Set AN/TPM-37 (T.O. 33D7-6-24-2).

T.O. 33D7-24-13-4

Test Set, Video Signal Processor AN/TPM-32

Figure 9-1 Power Supply 373350-1 breakdown will be incorporated into this IPB.

This page follows Title page

Reproduction for non-military use of the information or illustrations contained in this publication is not permitted without specific approval of the issuing service. The policy for use of Classified Publications is established for the Air Force in AFR 205-1.

Technical orders are normally distributed promptly after printing. Date(s) shown on the title page (lower right) are for identification only. This is not a distribution date. Processing time sometimes causes distribution to only appear to have been delayed.

LIST OF EFFECTIVE PAGES

INSERT LATEST CHANGED PAGES. DESTROY SUPERSEDED PAGES.

NOTE: The portion of the text affected by the changes is indicated by a vertical line in the outer margins of the page.

TOTAL NUMBER OF PAGES IN THIS MANUAL IS 44 CONSISTING OF THE FOLLOWING:

Page No.	Change No.
Title	0
A	0
i	0
ii (Blank)	0
1-1 - 1-8	0
2-1 - 2-25	0
2-26 (Blank)	0
3-1 - 3-2	0
4-1 - 4-3	0
4-4 (Blank)	0

Upon receipt of the second and subsequent changes to this technical order, personnel responsible for maintaining this publication in current status will ascertain that all previous changes have been received and incorporated. Action should be taken promptly if the publication is incomplete.

* The asterisk indicates pages changed, added, or deleted by the current change.

ADDITIONAL COPIES OF THIS PUBLICATION MAY BE OBTAINED BY USAF ACTIVITIES IN ACCORDANCE WITH T.O. 00-5-2.

USAF

LIST OF REVISED PAGES

The following pages in this Preliminary Technical Manual have been revised in accordance with information available as of 29 January 1972.

Title

B

1-1

2-5

2-7

2-9

2-11

2-14 - 2-15

2-18

2-20

3-1 - 3-2

TABLE OF CONTENTS

Section		Page
I	INTRODUCTION	1-1
II	GROUP ASSEMBLY PARTS LIST	
	Test Set, Video Signal Processor, AN/TPM-32	2-1
	Cable Assembly, Radio Frequency	2-3
	Cable Assembly, Multi-Pin	2-4
	Electrical Assembly, Video Signal Processor	2-6
	Panel Assembly, Video Signal Processor Test Set	2-11
	Circuit Card Assembly, 32 Indicator	2-13
	Circuit Card Assembly, 25 Indicator	2-14
	Circuit Card Assembly, 12 Indicator	2-15
	Power Plate Assembly	2-17
	Circuit Card Assembly (FCL)	2-18
	Circuit Card Assembly (CFF)	2-19
	Circuit Card Assembly (FSK)	2-20
	Circuit Card Assembly (GTT)	2-21
	Circuit Card Assembly (DDL)	2-22
	Circuit Card Assembly (GTD)	2-23
	Circuit Card Assembly (GCT)	2-24
	Circuit Card Assembly (DDS)	2-25
III	NUMERICAL INDEX	3-1
IV	REFERENCE DESIGNATION INDEX	4-1

SECTION I

INTRODUCTION

1-1. SCOPE

1-2. This Illustrated Parts Breakdown lists and illustrates all replaceable components, assemblies, and parts of Test Set, Video Signal Processor, AN/TPM-32, manufactured by AIL, a division of Cutler-Hammer, Inc., Deer Park, New York. The Illustrated Parts Breakdown has been prepared in accordance with specifications MIL-M-8910 and MIL-M-38730 and is to be used in conjunction with the Service Manual and the Circuit Diagrams Manual for the Video Signal Processor whenever service or repair is required. No TCTO's have been incorporated in this Illustrated Parts Breakdown. The equipment covered herein is configured for interservice DOD AIMS System use. Any changes affecting form, fit, or function shall be by Configuration Control Board Directive only. The technical manuals may be revised by or for the procuring activity without the approval of the Configuration Control Board in the following instances, providing form, fit, or function is not affected:

a. When the change consists of clarifying, expanding, correcting, or updating existing information on the technical manual.

b. When the item described in the technical manuals is no longer available and a substitute item must be used.

1-3. This Illustrated Parts Breakdown is contained in one volume and is divided into four sections as follows:

a. Section I, Introduction. This section contains the instructions you will need to use the information contained in Sections II, III, and IV correctly.

b. Section II, Group Assembly Parts List. All replaceable parts and assemblies required for maintenance are illustrated, listed and identified in this section.

c. Section III, Numerical Index. This section is a complete alphabetical-numerical index of all parts listed in Section II and provides a cross reference to the figure and index number that illustrates and identifies each part.

d. Section IV, Reference Designation Index. This section is a complete listing of all electronic parts by their reference designations, arranged in alphabetical-numerical order. The Reference Designation Index provides a cross reference to the part numbers and figure and index numbers in Sections II and III.

1-4. GROUP ASSEMBLY PARTS LIST

1-5. The Group Assembly Parts List contains a breakdown of all replaceable parts of the Video Signal Processor listed in the order of disassembly (where disassembly order is significant), beginning with the complete set, each major assembly, and finally breaking down into detailed subassemblies and parts.

1-6. Each item of the Group Assembly Parts List is arranged and indented to show its proper relationship to the unit of which it is a part and to the complete article. Each assembly listed is followed immediately (except for attaching parts) by its component parts, properly indented to show their relationship to the assembly.

1-7. Attaching parts are listed immediately following the part they attach and have the same indentation. They have the symbol (AP) immediately following the description.

1-8. An example of the next higher assembly relationship, indicated by indentation, is as follows:

1 2 3 4 5 6 7

MAIN ASSEMBLY
. ASSEMBLY
. SCREW (AP)
. NUT (AP)
. . SUBASSEMBLY
. . . SUB-SUBASSEMBLY

Change 1

1-9. Electronic components such as capacitors, coils, resistors, etc., are listed in groups according to type, under each assembly in which they occur. Parts of riveted or welded assemblies or wiring components that are normally procured in bulk are not listed.

1-10 Each detailed part is keyed to the illustration in which it is shown by means of a figure and index number, with the following exceptions:

a. Line Drawings. An assembly which is not shown assembled on a line drawing is not indexed. However, it is listed in the Group Assembly Parts List preceding its detailed parts (refer to paragraph 1-6).

b. Photographs. Hardware used as attaching parts for electronic items is not indexed on photographs. However, it is listed in the Group Assembly Parts List immediately following the part it attaches.

1-11. The Group Assembly Parts List is divided into five columns as follows:

a. FIG. AND INDEX NO. This column contains the figure and index numbers of illustrated items.

b. PART NUMBER. This column lists one of the following:

1. An AIL part number of an item manufactured by AIL.

2. The part number of a commercially manufactured item.

3. A government standard part number, such as AN or MS.

c. DESCRIPTION. This column identifies the item by one or more of the following means:

1. Approved Federal Item Identification name obtained from Cataloging Handbook H6-1.

2. Item name assigned by the manufacturer.

3. A manufacturer's code number is shown in parentheses following the description, as listed in the Cataloging Handbook H4-1. (Refer to paragraph 1-25.) When there is no manufacturer's code shown, the part is either an AIL part or a Government standard part.

4. The notation (see fig 0-00 for nha) is listed immediately following its description or vendor code of the number 1 ident item(s) of each figure, except figure 1. The figure number indicates the next higher assembly in which the item is physically located while the index number serves as a guide to locate the part within the next higher assembly.

d. UNITS PER ASSY. This column contains one of the following:

1. The exact quantity of the item as required for its immediate next higher assembly. (For example, if three dial knob assemblies are used on an electronic unit, and each knob assembly breaks down into one knob and two setscrews, the "units per assembly" is shown as one knob and two screws, the quantity required for one knob assembly only.)

2. The symbol AR for "as required". (These items are procured in bulk and used as required.)

3. The abbreviation Ref for "reference". (These items are listed for reference purposes only and Ref indicates that the quantity is listed in the next higher assembly in the Group Assembly Parts List, as indicated in the DESCRIPTION column.)

e. USABLE ON CODE. This column is left blank. When two (2) or more assemblies are contained in one figure, the differences are noted following the description of the parts with the notation "used on ---".

1-12. NUMERICAL INDEX

1-13. ARRANGEMENT. In the Numerical Index, manufacturer's part numbers are listed in alphabetical-numerical sequence in the PART NUMBER column. The order of precedence in the first column of the part number list is letters A through Z and the numerals 0 through 9. Alphabetical "O's" are considered to be numerical zeros. The order of precedence established by succeeding columns of the list is as follows:

Space (blank column)
Diagonal (slant)
Point (period)
Dash (-)
Letters A through Z
Numerals 0 through 9

1-14. FIGURE AND INDEX NUMBERS. The FIG. and INDEX NO. column in this section is a cross reference to the figure and index number of the applicable part, as listed in the Group Assembly Parts List (Section II). Those parts which have no assigned index number in Section II are listed in the Numerical Index by only the figure number followed by a dash. The figure and index number for Government (AN and MS) standard hardware is listed for first appearance only in the Group Assembly Parts List.

1-15. QUANTITY PER ARTICLE. The number in the QTY PER ART column is the quantity of the applicable part required for the complete Cable Adapter Set.

1-16. SOURCE CODES. All source codes available at the time this manual was prepared are shown in the SOURCE CODE column. Any source code received before the next change (or revision) to this publication will be included in that change (or revision). Policies, general information, and procedures for changing source and maintenance coding are contained in T.O. 00-25-195. Generally, the source codes and maintenance repair level codes herein (see Source Code and Repair Code columns) were assigned by Air Force personnel when this equipment was purchased. Assignment of codes was influenced by (a) maintenance policies, (b) predicted maintenance actions, (c) base facilities and capabilities, (d) economic considerations. Definitions of these codes follow.

a. Code "P" identifies parts which may be requisitioned and installed by any level of maintenance consistent with the activity's authorized scope of maintenance. Code "P" is applied to parts of which usage is anticipated or known. Restricted (emergency) service manufacture of code "P" items is considered practical but may be accomplished only after confirmation of nonavailability from supply sources.

b. Code "PD" identifies parts which may be requisitioned and installed by AF activities authorized depot-level maintenance only. Code "PD" is applied to parts on which usage is anticipated or known. Restricted (emergency) service manufacture of code "PD" parts is considered practical but may be accomplished only after confirmation of nonavailability from supply sources.

c. Code "P1" identifies parts which may be requisitioned and installed by any maintenance level consistent with the activity's authorized scope of maintenance. Code "P1" is applied to parts on which usage is anticipated or known, and which service manufacture is considered impractical.

d. Code "P1D" identifies parts which may be requisitioned and installed by AF activities authorized depot-level maintenance only. Code "P1D" is applied to parts on which usage is anticipated or known, and which service manufacture is considered impractical.

e. Code "P2" identifies insurance-type parts which can be installed by any activity within their authorized scope of maintenance. This code is applied to parts which have limited usage and are difficult, impractical or uneconomical to manufacture. These items are not subject to periodic replacement or wear-out. Infrequent replacement may result from deterioration or other unexpected occurrences. High reliability, long service life and delayed procurement items are included under this code.

f. Code "P2D" identifies insurance-type parts which may be installed by AF activities which are authorized depot-level maintenance only. This code is applied to parts as described under code "P2" and to delayed procurement items.

g. Code "M" identifies parts, the manufacture and installation of which are within the capabilities of field maintenance activities; and to which all of the following conditions apply:

1. Procurement is not justified because of low usage or peculiar storage and installation factors. Needs are to be met by local manufacture only as required.

2. Their manufacture does not require tools, equipment, or skills not normally authorized at field maintenance level.

3. Does not require test equipment not normally authorized at field maintenance level.

4. Does not require material not normally available in AF inventory.

h. Code "M" identifies parts which can be manufactured at activities authorized depot-level maintenance facilities and to which all of the following conditions apply:

1. Procurement is not justified because of low usage or peculiar storage and installation factors. The needs of base activities are to be met by requisitioning from the SSM or IM AMA.

2. Their manufacture is beyond capabilities of field maintenance activities as outlined above.

3. Their manufacture does not require tools or equipment not normally authorized by all AMA's.

i. Code "A" identifies items capable of being assembled at any level of maintenance and is applied to assemblies of two or more parts, the majority of which are purchased and/or service manufactured.

j. Code "A1" identifies assemblies which can be assembled at AF activities authorized depot-level maintenance only and is applied to assemblies described under "A" code.

k. Code "X" is applied to main structural members or similar parts, which, if required, would suggest extensive repair. The need for a part or parts coded "X" (wing spars, center section structure, etc.) should normally result in a recommendation to retire the article from service.

l. Code "X1" identifies parts applicable at any level of maintenance consistent with the activity's authorized scope of maintenance and for which it is more feasible to obtain the next higher assembly; for example, an integral detail part such as a welded segment inseparable from its assembly; a part machined in a matched set; or a part of any assembly which, if required, would suggest extensive reconditioning of such assembly. In some cases, code "X1" may be used to indicate an integral detail part of an assembly which has no anticipated usage and as an assembly was source coded "M" or "M1".

m. Code "X1D" identifies parts which are described under the "X1" code but which are applicable to AF activities authorized depot-level maintenance only.

n. Code "X2" identifies parts which are applicable to any level of maintenance consistent with the activity's authorized scope of maintenance, but which are impractical for service manufacture. This type of item will not be stocked. Such parts shall be obtained from reclamation or, if not available from this source, requisitioned through normal supply channels together with supporting justification for one-time procurement and immediate use. Repeated requests shall justify a change to a code "P1" or "P2", as applicable, if considered economical to procure and store such parts.

o. Code "X2D" identifies parts which are described under the "X2" code but which are applicable to AF activities authorized depot-level maintenance only. Repeated requests for such parts shall justify a change to a "P1D" or "P2D" code, as applicable, if considered economical and feasible to procure and stock such parts.

p. Code "U" identifies parts not procured, manufactured, or stocked. Code "U" is applied to installation drawings, diagrams, instruction sheets, field-service drawing numbers, and parts not otherwise of supply significance, including obsolete parts, which cannot be procured or service manufactured.

1-17. REPAIRABILITY CODES. All repairability codes available at the time this manual was prepared are shown in the REPAIR CODE column. Any repairability code received before the next change (or revision) to this publication will be included in that change (or revision). Repairability codes are assigned as follows:

a. CODE "A" -- NO REPAIR. Code "S" identifies items which are nonrepairable and have no reclamation value. When these items fail, they will be disposed of at user level as condemned material.

b. CODE "B" -- NO REPAIR: RECONDITION. Code "B" identifies assemblies or parts that will be reconditioned at the user level by adjusting, cleaning, soldering broken connections, etc. If these items cannot be returned to serviceable condition by such means, they will be disposed of at user level as condemned material. No repair parts or tools are specially procured for maintenance of these items.

c. CODE "F" -- REPAIR AT FIELD LEVEL. Code "F" identifies items which will be repaired by the field-level maintenance activities. Normal servicing will be done by organizational level maintenance. Selected tools and technical order data are procured and provided to applicable field-level maintenance activities for repair of these items. No SRA is established for these items. If the condition of these items is such that they cannot be returned to serviceable condition by the field-level maintenance activity with authorized parts and tools, they will be disposed of as condemned material. If repair of "F" coded items cannot be accomplished due to unavailability of authorized parts, tools, or other capability, the applicable SSM/IM will be so advised with request for disposition instructions. "F" coded critical items, regardless of

condition, will be returned to supply for disposition instructions from the applicable SSM/IM.

d. CODE "D" -- LIMITED FIELD REPAIR; DEPOT OVERHAUL. Code "D" identifies items on which a limited degree of repair can be accomplished by field-level maintenance activities. Normal servicing will be done at organizational level. SRA is established for overhaul of these items. A range of repair parts, tools and technical order data consistent with the capability of repair is procured and provided to applicable field maintenance activities. Because of the design characteristics and complexity of repair, the degree of repair which is authorized on these items at the field maintenance level is necessarily determined by the degree of technical skills required and the cost of special tools, special test equipment, spare parts, and the predicted frequency of failure. If these items cannot be returned to serviceable condition with authorized parts and tools, they will be returned to supply for shipment to the designated SRA.

e. CODE "DM" -- LIMITED FIELD REPAIR; MOBILE DEPOT OVERHAUL. Code "DM" identifies items to which all the conditions of code "D" apply except that repair beyond field capability will be done by the mobile depot activity (MDA). If the MDA cannot repair these items, disposition instructions will be requested from the IM.

f. CODE "L" -- DEPOT-LEVEL MAINTENANCE ONLY. Code "L" identifies items that will be repaired only at a designated SRA. Necessary parts, repair equipment, or overhaul capabilities are available at these activities. Required functional checkout and bench-check equipment may be provided to applicable organizational and field-level maintenance activities for accomplishing external adjustment or calibration and for verifying serviceability of these items. If they are found unserviceable, they will be turned in to supply for shipment to the SRA.

g. CODE "LM" -- DEPOT-LEVEL MAINTENANCE ONLY, MOBILE DEPOT ACTIVITY. Code "LM" identifies items to which all conditions of code "L" apply except that repair will be accomplished by the MDA. If the MDA cannot repair these items, disposition instructions will be requested from the IM.

1-18. REFERENCE DESIGNATION INDEX.

1-19. Reference designations are arranged in alphabetical-numerical sequence in the Reference Designation Index to permit rapid cross reference to the figure and index numbers of the assembly or subassembly in which the part appears. Reference designations are assigned to electrical and electronic parts in accordance with ASA Y32.16-1965, Electrical and Electronic Reference Designations, and consists of the following:

a. A numerical prefix to identify the unit, and for subassemblies, a subassembly letter and number which is followed by the part class and number. For example, the capacitor (C2) which is part of a Circuit Card Assembly GTD (A102) which is used on Test Set, Video Signal Processor (unit 18) is 18A102C2.

b. The reference designations shown in Section IV are the same as the reference designations shown in the Field Maintenance Manual T.O.

1-20. EXPLANATION OF TERMS, ABBREVIATIONS, AND SYMBOLS.

1-21. Terms, abbreviations, and symbols used in this IPB are as follows:

a. The notation "see fig-for nha" (following the description of a part indicates the "next higher assembly" of that part.

b. The notation "see fig-for breakdown" following the description of a part indicates that the item and its component parts are shown in detail in the figure indicated.

c. The notation "used on" following the description of a part indicates that the item is only used on the assembly indicated.

d. All abbreviations found in MIL-STD-12 as well as nonstandard abbreviations appearing in this Illustrated Parts Breakdown are listed below.

ABBREVIATION	DEFINITION
AP	attaching part
fig	figure
nha	next higher assembly
pn	part number
Ref	reference
Spec	specification
thru	through

1-22. PART NUMBERS AND MANUFACTURER'S CODES

1-23. AIL part numbers consist of a basic six-digit number suffixed by a dashed number or numbers which may designate a similar part or left- and right-hand parts, etc.

1-24. Purchased parts that are used on this equipment are listed under the manufacturer's number and are procurable through normal commercial sources.

1-25. The manufacturer's code number shown in the DESCRIPTION column in Section II is the Federal Supply Code for Manufacturers, obtained from Cataloging Handbook H4-1. Manufacturer's codes used in this publication are as follows:

CODE NO.	VENDOR NAME & ADDRESS
00752	AIL, a division of Cutler-Hammer Comac Road Deer Park, N.Y. 11729
08524	Deutsch Fastener Corp. Los Angeles, Calif.
12324	Stake Fastener Co. 1710 N. Potrero Ave. South El Monte, Calif. 91733
13103	Thermalloy Co. 8717 Diplomacy Row Dallas, Tex. 75247
19178	Zero Mfg. Co., East Division 288 Main Street Monson, Mass. 01057
26365	Gries Reproducer Corp. 125 Beechwood Ave. New Rochelle, N.Y. 10802
52147	Milton Roy Co. 1313 E. Mermaid Lane Philadelphia, Pa. 19146
71279	Cambridge Thermionic Corp. 445 Concord Ave. Cambridge, Mass. 02138
72794	Dzus Fastener Co., Inc. 425 Union Blvd. West Islip, N.Y. 11795
78769	Titchener, E.H. and Co. 1 Titchener Place Binghamton, N.Y. 13902
79963	Zierick Mfg. Co. Radio Circle Mt. Kisco, N.Y. 10549
94222	South Chester Corp. Chester, Pa.
94375	Automatic Metal Products Corp. 313-315 Berry St. Brooklyn, N.Y. 11211
97954	U.S. Components Inc. 1320 Zerega Ave. Bronx, N.Y. 10462
98410	ETC, Inc. 990 E. 67th St. Cleveland, Ohio 44103

1-26. IDENTIFICATION OF PARTS.

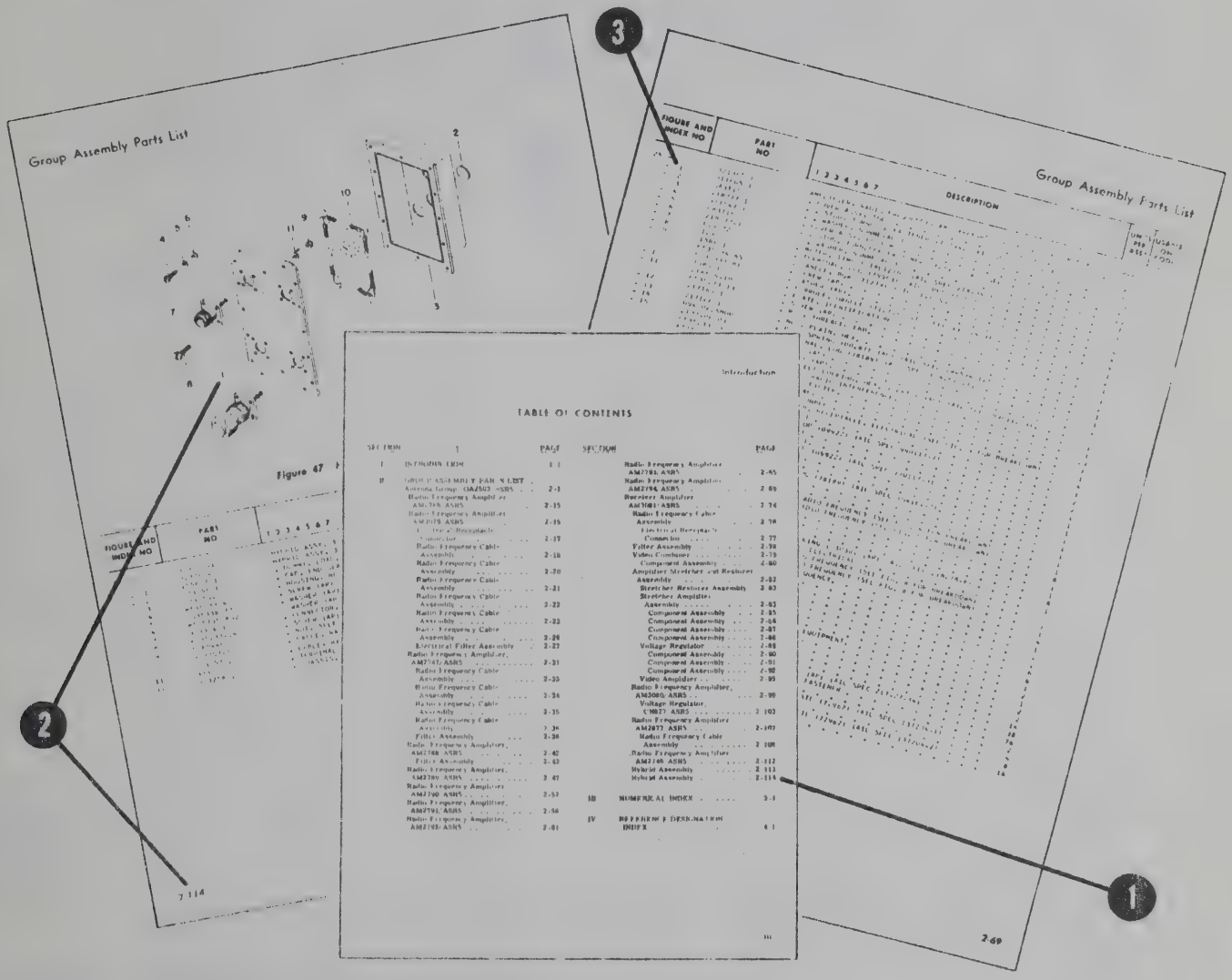
1-27. To find the part number of a part, proceed as follows:

a. Look in the Table of Contents for the figure number of the group assembly to which the part belongs.

b. Turn to the figure, find the illustration of the part, and note its index number.

c. Turn to the Group Assembly Parts List that corresponds to the figure, find the index number of the part, and the desired part number will be found.

HOW TO USE THE ILLUSTRATED PARTS BREAKDOWN



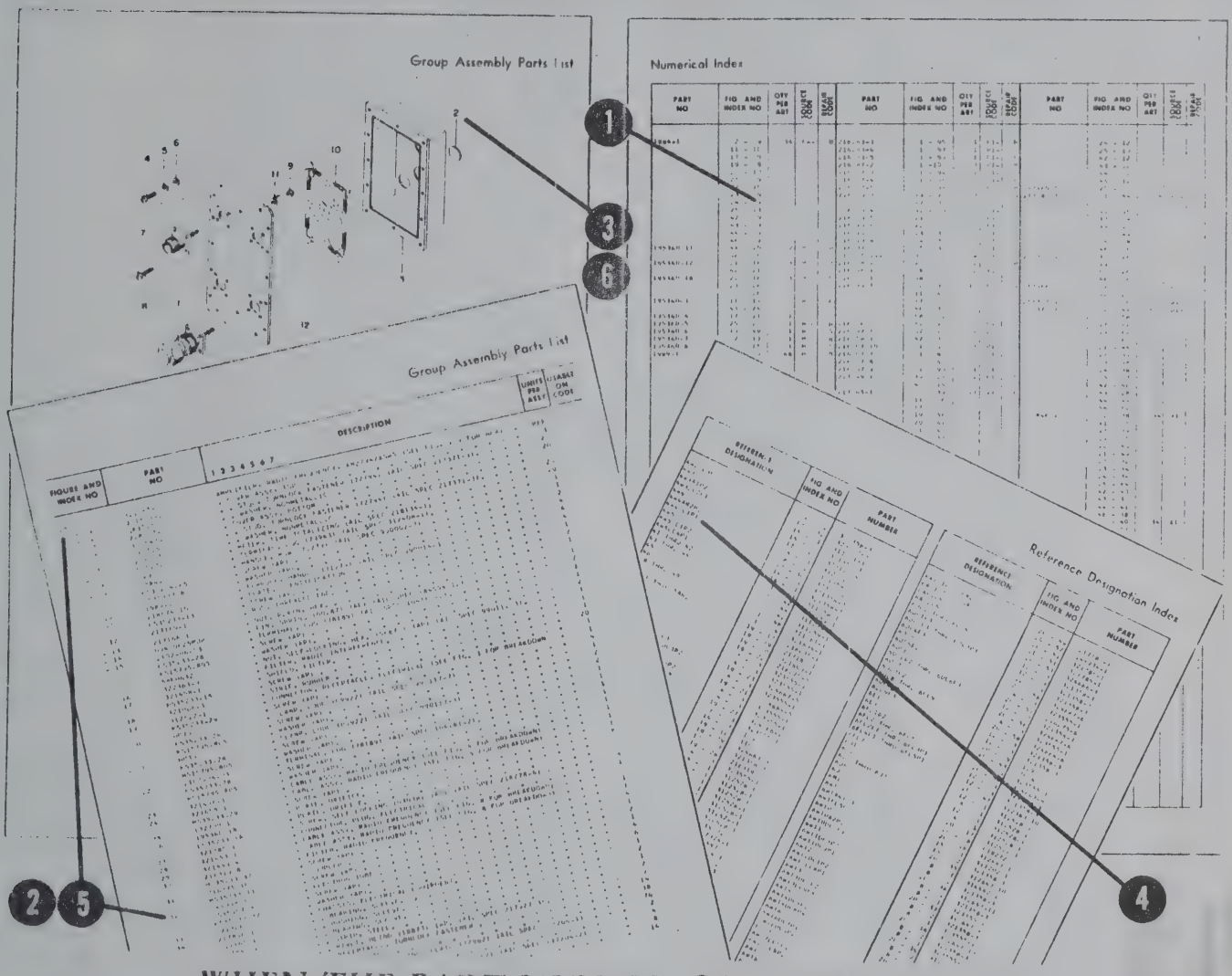
WHEN THE PART NUMBER IS NOT KNOWN

1. Determine the function and application of the part required. Turn to the Table of Contents and select the most appropriate title. Note the illustration number.

2. Turn to the page indicated and locate the desired part on the illustration.

3. From the illustration, obtain the index number assigned to the part desired. Refer to the accompanying description for specific information regarding the part.

HOW TO USE THE ILLUSTRATED PARTS BREAKDOWN



WHEN THE PART NUMBER OR REFERENCE DESIGNATION IS KNOWN

1. When the part number is known, refer to the Numerical Index. Locate the part number and note the figure and index number assigned to the part number.

2. Turn to the figure number indicated and locate the index number referenced in the Numerical Index.

3. If a pictorial representation of the part, or its location is desired, refer to the same index number on the accompanying illustration.

4. When the reference designation is known, refer to the Reference Designation Index. Locate the reference designation and note the figure and index number and the part number assigned.

5. Turn to the figure indicated and locate the index number referenced in the Reference Designation Index.

6. If a pictorial representation of the part, or its location is desired, refer to the same index number on the accompanying illustration.

SECTION II

GROUP ASSEMBLY PARTS LIST

FIG. AND INDEX NO.	PART NUMBER	1 2 3 4 5 6 7 DESCRIPTION	UNITS PER ASSY	USABLE ON CODE
1-	374571-1	TEST SET, Video signal processor AN/TPM-32	1	
	387585-1	. PLUG ASSEMBLY, Test lead	1	
-1	387459-1	. . JACK, Tip	2	
-2	387165-1	. CABLE ASSEMBLY, Radio frequency (see fig 2 for breakdown)	1	
-3	387167-1	. CABLE ASSEMBLY, Multi-pin (see fig 3 for breakdown)	1	
	387168-1	. CABLE ASSEMBLY, Multi-pin (see fig 3 for breakdown)	1	
	387169-1	. CABLE ASSEMBLY, Multi-pin (see fig 3 for breakdown)	1	
	387170-1	. CABLE ASSEMBLY, Multi-pin (see fig 3 for breakdown)	1	
-4	1733	. CARD EXTRACTOR (78769) (AIL spec 385546-1)	1	
-5	386041-1	. ELECTRICAL ASSEMBLY, Video signal processor test set (see fig 4 for breakdown)	1 1	
-6	D9597-1	. CASE, Combination (19178) (AIL spec 386507-1)	1	

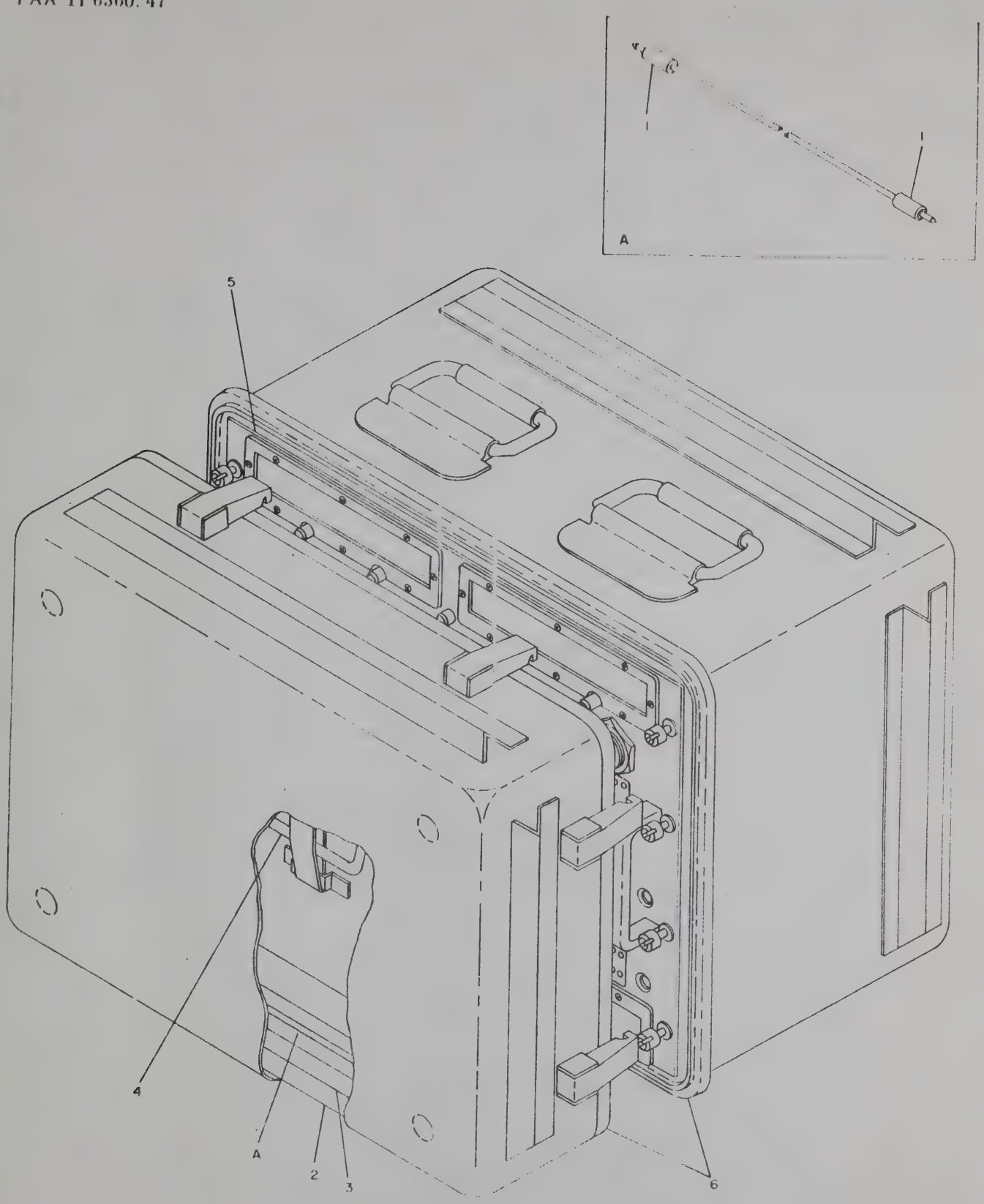


Figure 1. Video Signal Processor Test Set AN/TPM-32

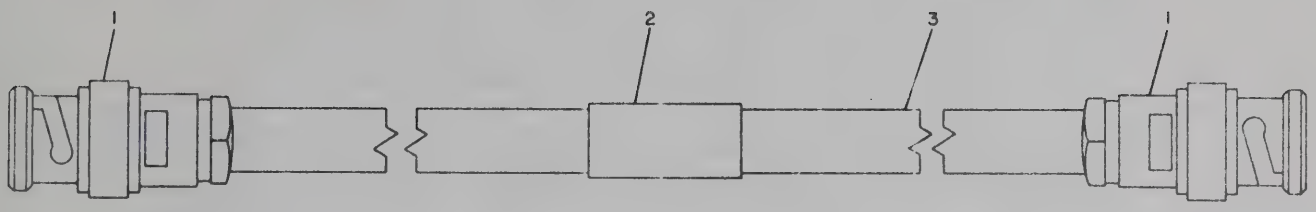


Figure 2. Radio Frequency Cable Assembly

FIG. AND INDEX NO.	PART NUMBER	1 2 3 4 5 6 7 DESCRIPTION	UNITS PER ASSY	USABLE ON CODE
2-	387165-1	CABLE ASSEMBLY, Radio frequency (see fig 1-2 for nha)	Ref	
-1	385944-1	. CONNECTOR, Plug, electrical	2	
-2	387342-1	. BAND, Marker, cable	1	
-3	RG179BU	. CABLE	AR	

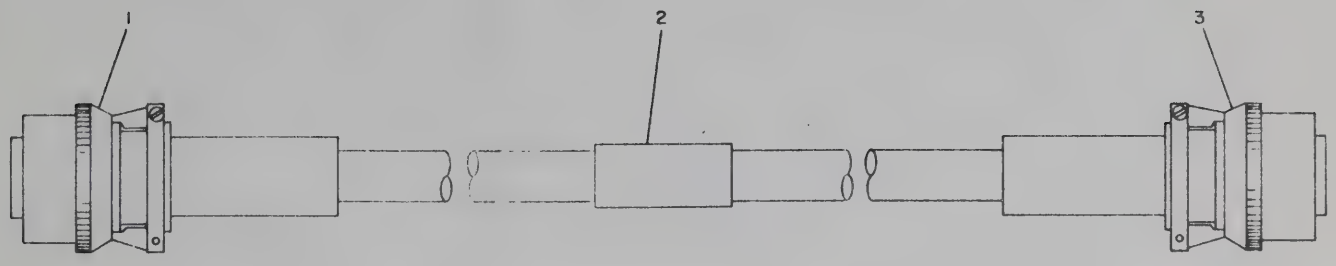


Figure 3. Multi-Pin Cable Assembly

FIG. AND INDEX NO.	PART NUMBER	1 2 3 4 5 6 7 DESCRIPTION	UNITS PER ASSY	USABLE ON CODE
3-	387167-1	CABLE ASSEMBLY, Multi-pin (see fig 1-3 for nha)	Ref	
	387168-1	CABLE ASSEMBLY, Multi-pin (see fig 1-3 for nha)	Ref	
	387169-1	CABLE ASSEMBLY, Multi-pin (see fig 1-3 for nha)	Ref	
	387170-1	CABLE ASSEMBLY, Multi-pin (see fig 1-3 for nha)	Ref	
-1	MS3126F14-5S	. CONNECTOR (used on 387167-1)	1	
	MS3126F18-11S	. CONNECTOR (used on 387168-1)	1	
	MS3126F20-41S	. CONNECTOR (used on 387169-1)	1	
	MS3126F22-55S	. CONNECTOR (used on 387170-1)	1	
-2	387342-3	. BAND, Marker (used on 387167-1)	1	
	387342-4	. BAND, Marker (used on 387168-1)	1	
	387342-5	. BAND, Marker (used on 387169-1)	1	
	387342-6	. BAND, Marker (used on 387170-1)	1	
-3	UP221M	. CONNECTOR (used on 387167-1 and 387168-1)	1	
	MS3126F20-41P	. CONNECTOR (used on 387169-1)	1	
	MS3126F22-55P	. CONNECTOR (used on 387170-1)	1	

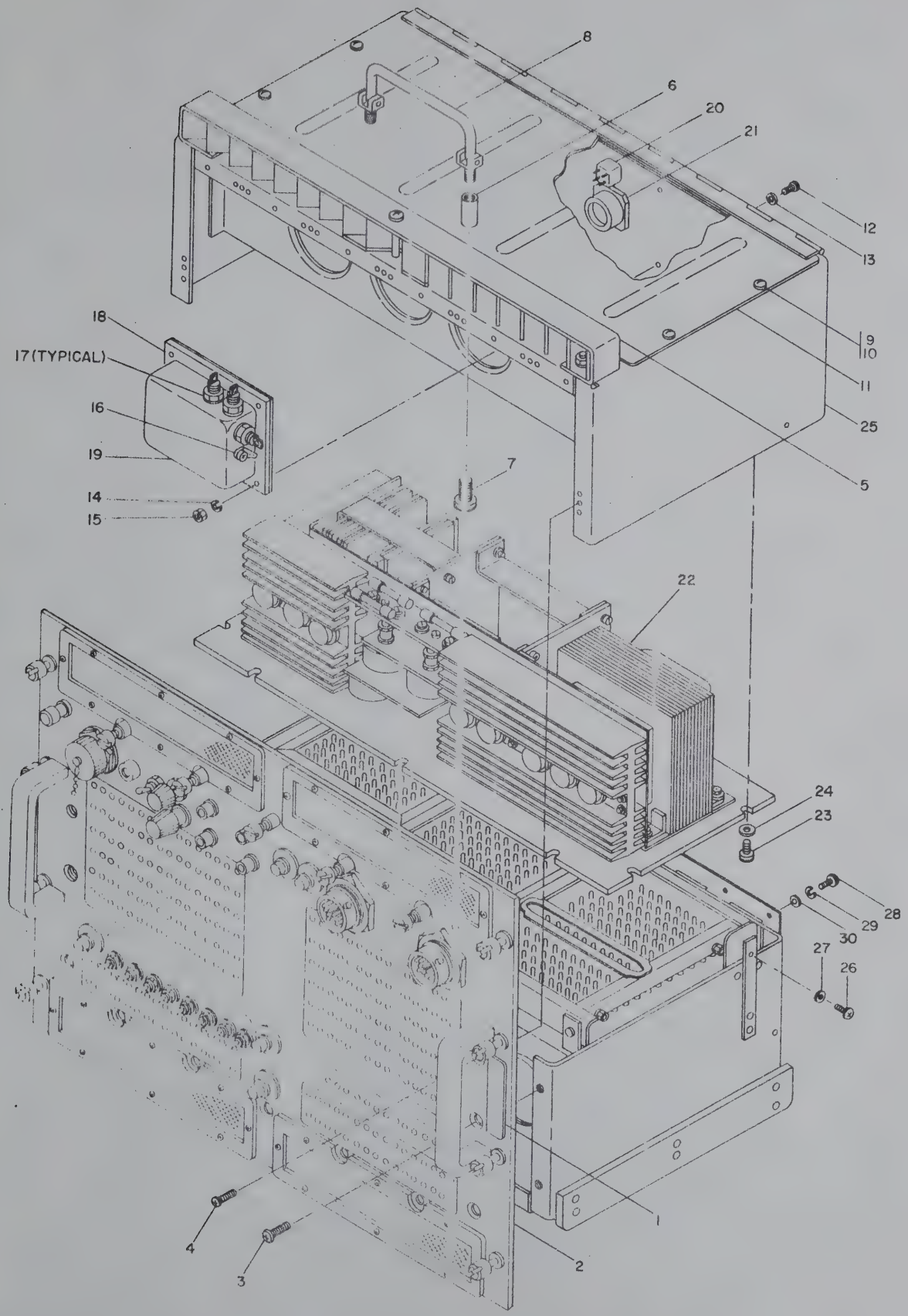


Figure 4. Video Signal Processor Test Set Electrical Assembly (Sheet 1) ~~of 2~~

Change 1

FIG. AND INDEX NO.	PART NUMBER	1 2 3 4 5 6 7 DESCRIPTION	UNITS PER ASSY	USABLE ON CODE
4-	386041-1	ELECTRICAL ASSEMBLY, Video signal processor test set (see fig 1-5 for nha)	Ref	
-1	NO NUMBER	. NAMEPLATE	1	
-2	386021-1	. PANEL ASSEMBLY, BRP Test set (see fig 5 for breakdown)	1	
-3	SFSW8C8DS01BK	. SCREW (AP) (12324) (AIL spec 374654-1)	9	
-4	MS51957-126	. SCREW (AP)	2	
-5	387015-1	. LOUVER ASSEMBLY	1	
	M851957-37	. SCREW (AP)	1	
	MS15795-805	. WASHER (AP)	1	
	MS35338-136	. WASHER (AP)	1	
	MS35649-264	. NUT (AP)	1	
	MS51957-17	. SCREW (AP)	4	
	MS15795-803	. WASHER (AP)	4	
	MS35338-135	. WASHER (AP)	4	
	MS35649-244	. NUT (AP)	4	
-6	387182-1	. STANDOFF, Handle	2	
-7	MS51958-92	. SCREW (AP)	2	
-8	317841-1	. HANDLE, Door	1	
	386115-1	. COVER ASSEMBLY, Upper chassis	1	
	MS51957-16	. SCREW (AP)	7	
	MS15795-803	. WASHER (AP)	7	
-9	3SS	. . RING, Retaining (72794) (AIL spec 363218-1)	7	
-10	AJ3-30SS	. . STUD, Turnbutton fastener (72794) (AIL spec 363216-2)	7	
-11	386114-2	. . COVER	1	
	386106-1	. FILTER ASSEMBLY	1	
-12	MS51957-17	. SCREW (AP)	4	
-13	MS15795-803	. WASHER (AP)	4	
-14	MS35338-135	. WASHER (AP)	4	
-15	MS35649-264	. NUT (AP)	4	
-16	371956-1	. . TERMINAL, Lug	1	
	MS51957-1	. . SCREW (AP)	1	
	MS15795-807	. . WASHER (AP)	1	
	370782-3	. . NUT (AP)	1	
-17	385598-1	. . FILTER, Radio interference	4	
-18	371132-1	. . GASKET	1	
-19	386105-1	. . CHASSIS	1	
-20	MS24656-231	. SWITCH	1	
-21	MS3124E14-5P	. CONNECTOR	1	
-22	387076-1	. POWER PLATE ASSEMBLY (see fig 9 for breakdown)	1	
-23	MS51957-30	. SCREW (AP)	10	
-24	MS15795-805	. WASHER (AP)	10	
-25	386030-1	. CHASSIS	1	
-26	386260-1	. SCREW (AP)	2	
-27	MS35338-136	. WASHER (AP)	2	

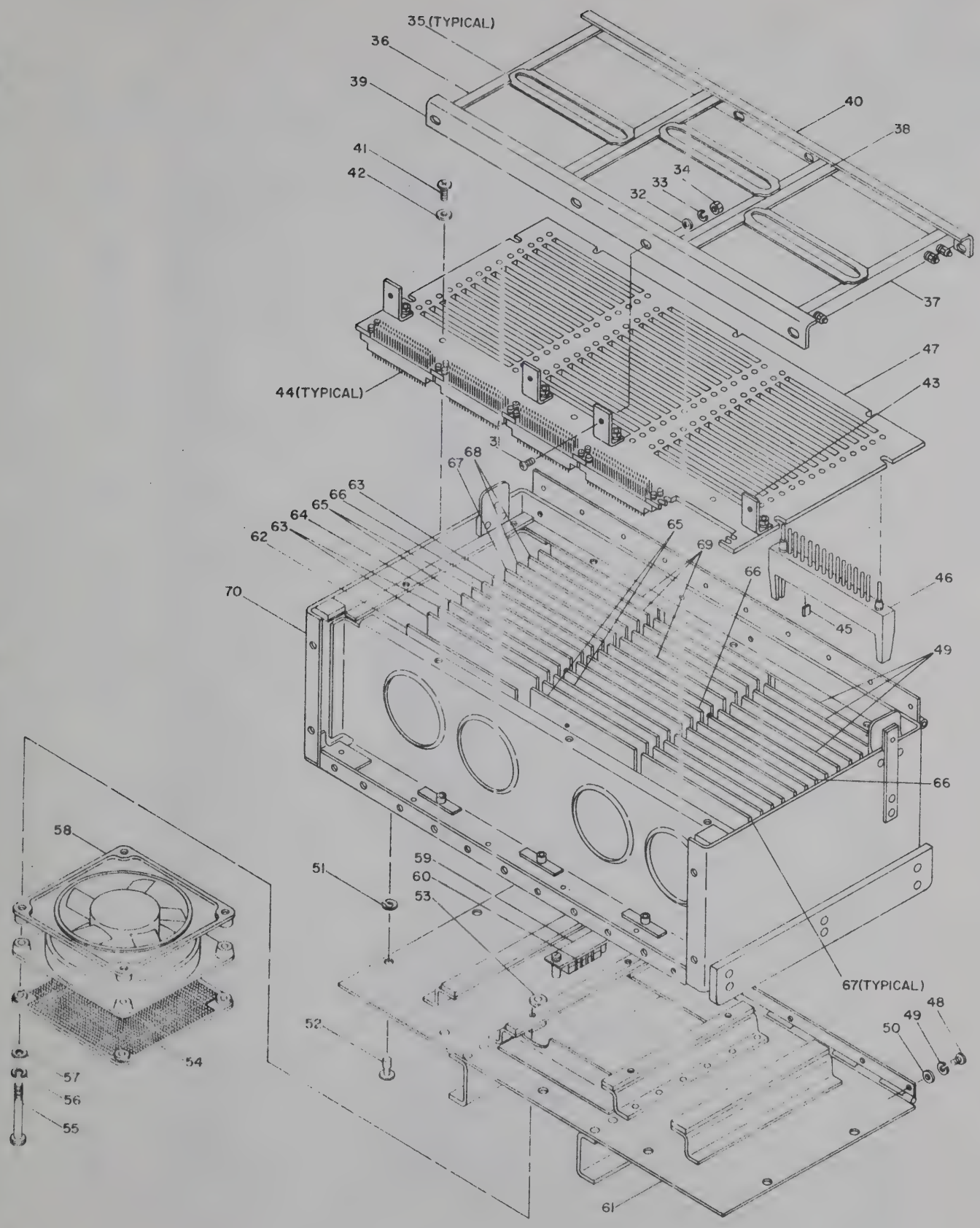


Figure 4. Video Signal Processor Test Set Electrical Assembly (Sheet 2 ~~of 2~~)

Change 1

FIG. AND INDEX NO.	PART NUMBER	1 2 3 4 5 6 7 DESCRIPTION	UNITS PER ASSY	USABLE ON CODE
4-28	MS51957-14	. SCREW (AP)	10	
-29	MS15795-803	. WASHER (AP)	10	
-30	MS35338-135	. WASHER (AP)	10	
	386136-1	. WIRE GUIDE ASSEMBLY	1	
-31	MS51957-16	. SCREW (AP)	4	
-32	MS15795-803	. WASHER (AP)	4	
-33	MS35338-135	. WASHER (AP)	4	
-34	MS35649-244	. NUT (AP)	4	
-35	373868-1	. . GUIDE	3	
-36	386131-1	. . RAIL	1	
-37	386133-1	. . RAIL	1	
	MS51957-15	. . SCREW (AP)	8	
	MS15795-803	. . WASHER (AP)	16	
	MS35338-135	. . WASHER (AP)	8	
	MS35649-244	. . NUT (AP)	8	
-38	386132-1	. . RAIL	2	
	MS51957-16	. . SCREW (AP)	8	
	MS15795-803	. . WASHER (AP)	16	
	MS35338-135	. . WASHER (AP)	8	
	MS35649-244	. . NUT (AP)	8	
-39	386134-1	. . CHANNEL	1	
-40	386135-1	. . CHANNEL	1	
	386090-1	. CONNECTOR PLATE ASSEMBLY	1	
-41	MS51957-30	. SCREW (AP)	12	
-42	MS15795-805	. WASHER (AP)	12	
-43	386250-1	. . BRACKET	4	
	MS51959-16	. . SCREW (AP)	8	
	MS15795-803	. . WASHER (AP)	8	
	MS35338-135	. . WASHER (AP)	8	
	MS35649-244	. . NUT (AP)	8	
-44	GR100MISLWWP	. . CONNECTOR (97954) (AIL spec 374694-3)	4	
	386056-1	. . CONNECTOR PLATE ASSEMBLY	1	
-45	374118-1	. . . KEY, Polarizing	88	
-46	372215-1	. . . CONNECTOR	42	
-47	386055-1	. . . PLATE, Connector	1	
	386002-1	. COVER ASSEMBLY, Lower chassis	1	
-48	MS51957-14	. SCREW (AP)	7	
-49	MS15795-803	. WASHER (AP)	7	
-50	MS35338-135	. WASHER (AP)	7	
-51	3SS	. . RING, Retaining (72794) (AIL spec 363218-1)	7	
-52	AJ3-35SS	. . STUD, Turnbutton fastener (72794) (AIL spec 363216-3)	7	
-53	MS35489-4	. . GROMMET	2	
-54	385055-1	. . GUARD, Fan	1	
-55	385056-3	. . SCREW (AP)	4	
-56	MS35338-136	. . WASHER (AP)	4	

FIG. AND INDEX NO.	PART NUMBER	1 2 3 4 5 6 7 DESCRIPTION	UNITS PER ASSY	USABLE ON CODE
4-57	MS15795-805	. . WASHER (AP)	4	
-58	374117-3	. . FAN, Tube axial	1	
-59	386004-1	. . STRIP	1	
	MS51957-17	. . SCREW (AP)	2	
	MS35338-135	. . WASHER (AP)	2	
	MS15795-803	. . WASHER (AP)	2	
-60	33003-714	. . TERMINAL BOARD (98410) (AIL spec 990270-2)	1	
	MS51957-16	. . SCREW (AP)	4	
	MS15795-803	. . WASHER (AP)	4	
	MS35338-135	. . WASHER (AP)	4	
	MS35649-244	. . NUT (AP)	4	
-61	386003-1	. . COVER	1	
-62	374262-1	. CIRCUIT CARD ASSEMBLY (FCL) (see fig 10 for breakdown)	1	
-63	373621-1	. CIRCUIT CARD ASSEMBLY (CFF) (see fig 11 for breakdown)	3	
-64	374059-1	. CIRCUIT CARD ASSEMBLY (FSK) (see fig 12 for breakdown)	1	
-65	373361-1	. CIRCUIT CARD ASSEMBLY (GTT) (see fig 13 for breakdown)	4	
-66	373298-1	. CIRCUIT CARD ASSEMBLY (DDL) (see fig 14 for breakdown)	3	
-67	373296-1	. CIRCUIT CARD ASSEMBLY (GTD) (see fig 15 for breakdown)	18	
-68	373359-1	. CIRCUIT CARD ASSEMBLY (GCT) (see fig 16 for breakdown)	2	
-69	373673-1	. CIRCUIT CARD ASSEMBLY (DDS) (see fig 17 for breakdown)	6	
-70	385987-1	. CHASSIS ASSEMBLY, Lower	1	

Change 1

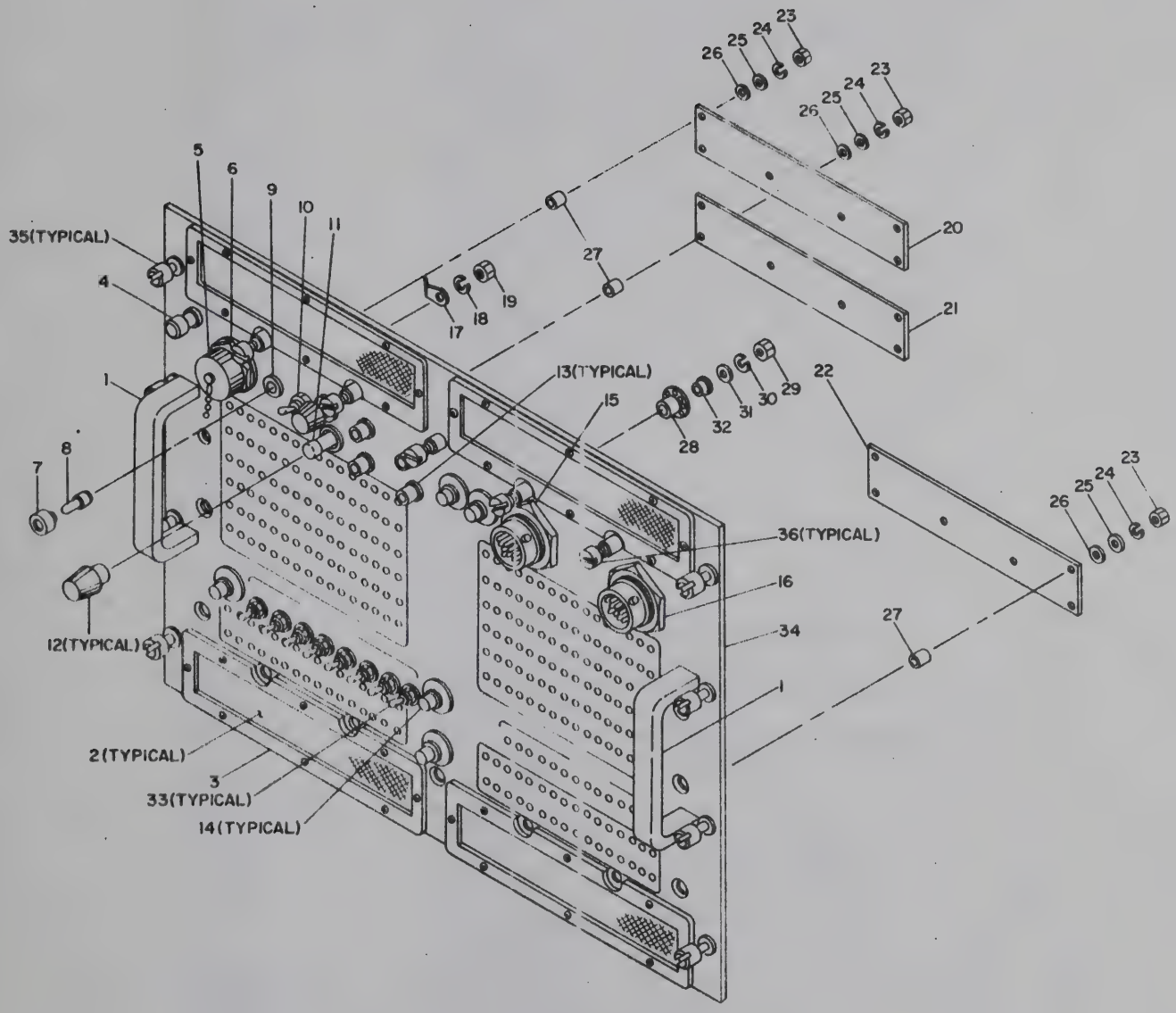


Figure 5. Video Signal Processor Test Set Panel Assembly

FIG. AND INDEX NO.	PART NUMBER	1 2 3 4 5 6 7 DESCRIPTION	UNITS PER ASSY	USABLE ON CODE
5-	386021-1	PANEL ASSEMBLY, Video signal processor test set (see fig 4-2 for nha)	Ref	
-1	386040-1	. HANDLE	2	
	MS24693C51	. SCREW (AP)	4	
	386576-1	. SCREEN AND FRAME ASSEMBLY	4	
	374654-7	. SCREW (AP)	32	
-2	386045-1	. . SCREEN	1	
-3	386116-1	. . FRAME	1	
-4	PB05NC01	. POST	1	
	MS51959-261	. SCREW (AP)	1	
-5	371693-3	. COVER, Connector	1	
-6	MS3122E14-5P	. CONNECTOR	1	
-7	LC13WT2	. LENS	1	
-8	MS25252C7A	. LAMP	1	
-9	LH74-1	. LAMPHOLDER	1	
-10	MS35059-23	. SWITCH	1	
-11	F02A125V3AS	. FUSE	2	
-12	FHN26G	. FUSEHOLDER	2	
-13	M39012-21-003	. CONNECTOR	4	
-14	MS25089-3C	. SWITCH	5	
-15	MS3124E20-41P	. CONNECTOR	1	
-16	MS3124E22-55P	. CONNECTOR	1	
-17	626-4	. TERMINAL, Lug (79963) (AIL spec 990205-1)	1	
-18	MS35649-244	. NUT (AP)	1	
-19	MS35338-135	. WASHER (AP)	1	
-20	385883-1	. CIRCUIT CARD ASSEMBLY, 32 Indicator (see fig 6 for breakdown)	7	
-21	385992-1	. CIRCUIT CARD ASSEMBLY, 25 Indicator (18A3) (see fig 7 for breakdown)	1	
-22	385995-1	. CIRCUIT CARD ASSEMBLY, 12 Indicator (18A8) (see fig 8 for breakdown)	1	
-23	MS35649-244	. NUT (AP)	54	
-24	MS35338-135	. WASHER (AP)	54	
-25	MS15795-803	. WASHER (AP)	54	
-26	972-301	. WASHER (AP) (26365) (AIL spec 990114-1)	54	
-27	386268-1	. SPACER	54	
-28	1038-1	. STUD, Grounding (71279) (AIL spec 990313-2)	2	
-29	MS35649-244	. NUT (AP)	2	
-30	MS35338-135	. WASHER (AP)	2	
-31	MS15795-803	. WASHER (AP)	2	
-32	974-302	. BUSHING (26365) (AIL spec 990049-1)	2	

Change

FIG. AND INDEX NO.	PART NUMBER	1 2 3 4 5 6 7 DESCRIPTION	UNITS PER ASSY	USABLE ON CODE
5-33	MS24655-231	. SWITCH	8	
	374656-1	. NUT (AP)	8	
	374655-1	. WASHER (AP)	8	
-34	386005-1	. PANEL ASSEMBLY	1	
-35	FRB7500-10B4	. . STUD, Turnlock fastener (08524) (AIL spec 374647-8)	8	
-36	53-17-711-24	. . FASTENER (94222) (AIL spec 323490-2)	5	

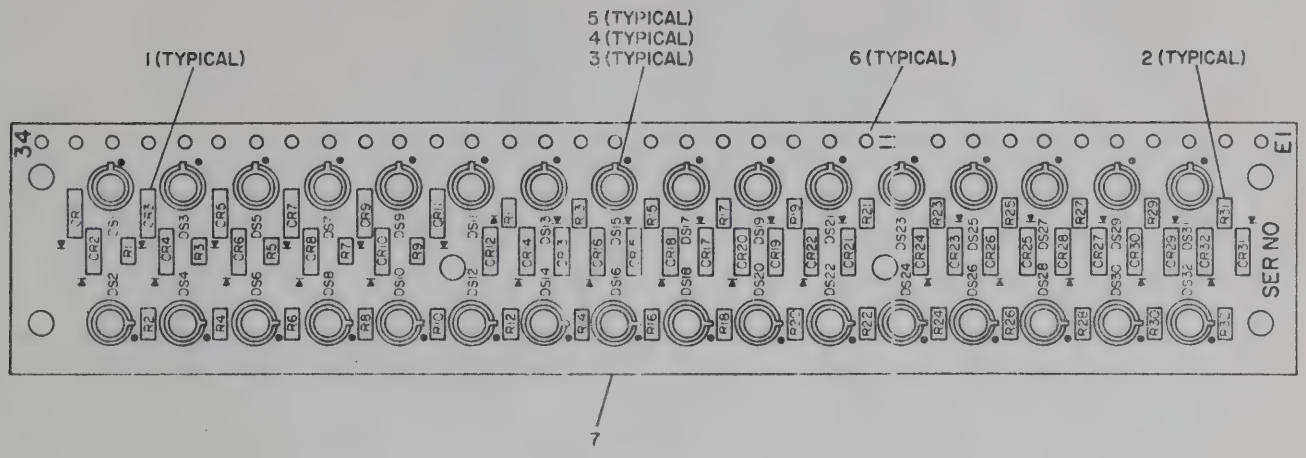


Figure 6. 32 Indicator Circuit Card Assembly

FIG. AND INDEX NO.	PART NUMBER	1 2 3 4 5 6 7 DESCRIPTION	UNITS PER ASSY	USABLE ON CODE
6-	385883-1	CIRCUIT CARD ASSEMBLY, 32 Indicator (see fig 5-20 for nha)	Ref	
-1	JAN1N4148	. SEMICONDUCTOR DEVICE	32	
-2	RCR05G301JS	. RESISTOR.	32	
-3	385595-1	. SEMICONDUCTOR DEVICE, Diode	32	
-4	10382DAP	. PAD (52147) (AIL spec 385907-1)	32	
-5	7717-149DAP	. PAD (13103) (AIL spec 385908-1)	32	
-6	1941-2-01	. TERMINAL (71279) (AIL spec 387358-1)	34	
-7	385882-1	. PRINTED CIRCUIT BOARD	1	

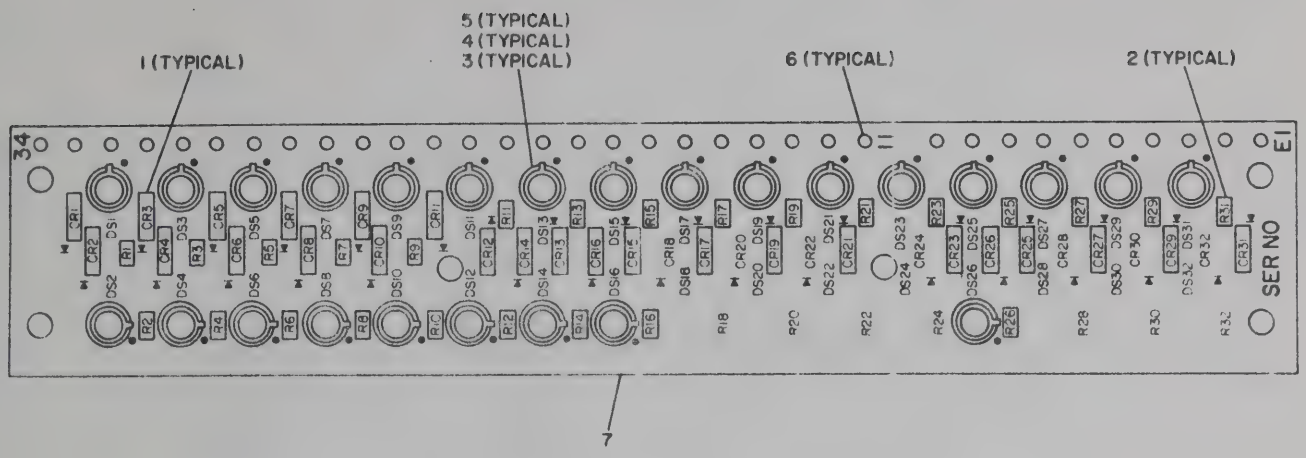


Figure 7. 25 Indicator Circuit Card Assembly (18A3)

FIG. AND INDEX NO.	PART NUMBER	1 2 3 4 5 6 7 DESCRIPTION	UNITS PER ASSY	USABLE ON CODE
7-	385992-1	CIRCUIT CARD ASSEMBLY, 25 Indicator (18A3) (see fig 5-21 for nha)	Ref	
-1	JAN1N4148	. SEMICONDUCTOR DEVICE	25	
-2	RCR05G301JS	. RESISTOR	25	
-3	385595-1	. SEMICONDUCTOR DEVICE, Diode	25	
-4	10382DAP	. PAD (52147) (AIL spec 385907-1)	25	
-5	7717-149DAP	. PAD (13103) (AIL spec 385908-1)	25	
-6	1941-2-01	. TERMINAL (71279) (AIL spec 387358-1)	34	
-7	385882-1	. PRINTED CIRCUIT BOARD	1	

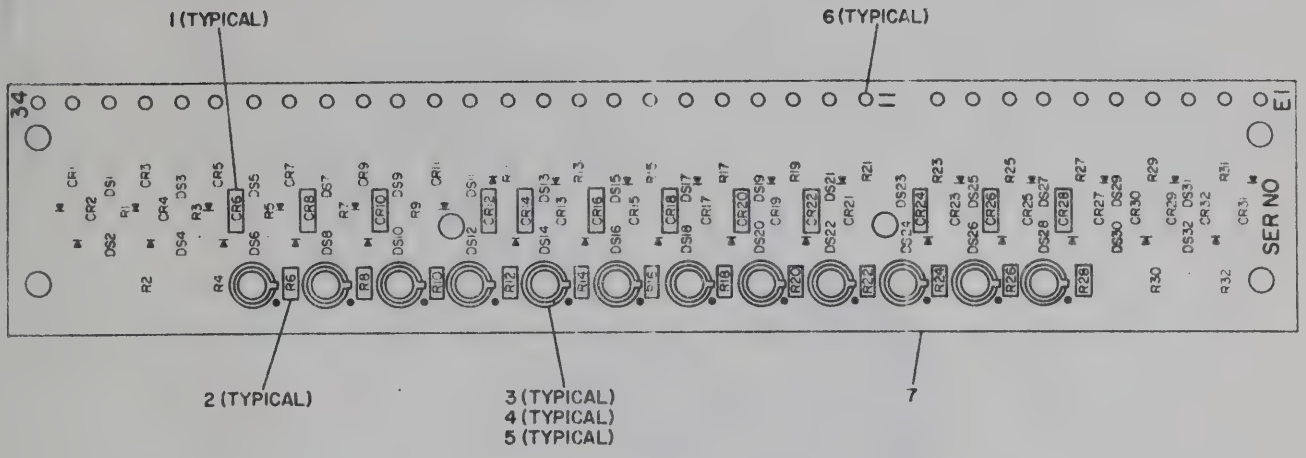


Figure 8. 12 Indicator Circuit Card Assembly (18H8)

FIG. AND INDEX NO.	PART NUMBER	1 2 3 4 5 6 7 DESCRIPTION	UNITS PER ASSY	USABLE ON CODE
8-	385995-1	CIRCUIT CARD ASSEMBLY, 12 Indicator (18H8) (see fig 5-22 for nha)	Ref	
-1	JAN1N4148	. SEMICONDUCTOR DEVICE	12	
-2	RCR05G301JS	. RESISTOR.	12	
-3	385595-1	. SEMICONDUCTOR DEVICE, Diode	12	
-4	10382DAP	. PAD (52147) (AIL spec 385907-1)	12	
-5	7717-149DAP	. PAD (13103) (AIL spec 385908-1)	12	
-6	1941-2-01	. TERMINAL (71279) (AIL spec 387358-1)	34	
-7	385882-1	. PRINTED CIRCUIT BOARD	1	

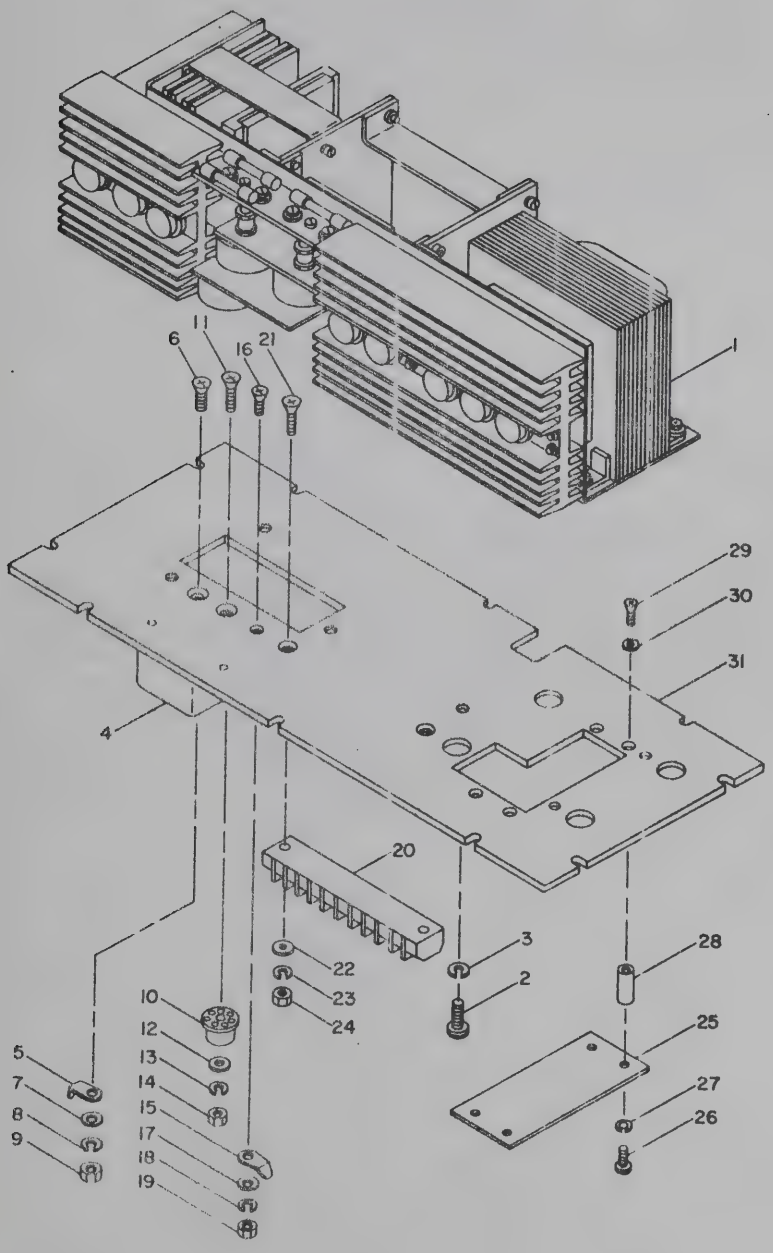


Figure 9. Power Plate Assembly

FIG. AND INDEX NO.	PART NUMBER	1 2 3 4 5 6 7 DESCRIPTION	UNITS PER ASSY	USABLE ON CODE
9-	387076-1	POWER PLATE ASSEMBLY (see fig 4-22 for nha)	Ref	
-1	373350-1	. POWER SUPPLY, Signal processor	1	
-2	MS51958-64	. SCREW (AP)	6	
-3	MS35338-138	. WASHER (AP)	6	
-4	CH53B1NF105M	. CAPACITOR	1	
	MS51957-29	. SCREW (AP)	2	
-5	805-8	. TERMINAL, Lug (79963) (AIL spec 990209-3)	1	
-6	MS51959-45	. SCREW (AP)	1	
-7	MS15795-807	. WASHER (AP)	1	
-8	MS35338-137	. WASHER (AP)	1	
-9	MS35649-284	. NUT (AP)	1	
-10	1039-1	. STUD, Grounding (71279) (AIL spec 990313-1)	1	
-11	MS51959-32	. SCREW (AP)	1	
-12	MS15795-805	. WASHER (AP)	1	
-13	MS35338-136	. WASHER (AP)	1	
-14	MS35649-264	. NUT (AP)	1	
-15	805-4	. TERMINAL, Lug (79963) (AIL spec 990209-1)	1	
-16	MS51959-16	. SCREW (AP)	1	
-17	MS15795-803	. WASHER (AP)	1	
-18	MS35338-135	. WASHER (AP)	1	
-19	MS35649-244	. NUT (AP)	1	
-20	8TB10	. TERMINAL BOARD	1	
-21	MS51959-32	. SCREW (AP)	2	
-22	MS15795-805	. WASHER (AP)	2	
-23	MS35338-136	. WASHER (AP)	2	
-24	MS35649-264	. NUT (AP)	2	
-25	386614-1	. STRIP, Protective	1	
-26	MS51957-14	. SCREW (AP)	4	
-27	MS15795-803	. WASHER (AP)	4	
-28	990031-42	. NUT, Sleeve	4	
-29	MS51959-14	. SCREW (AP)	4	
-30	MS35338-135	. WASHER (AP)	4	
-31	386137-1	. PLATE	1	

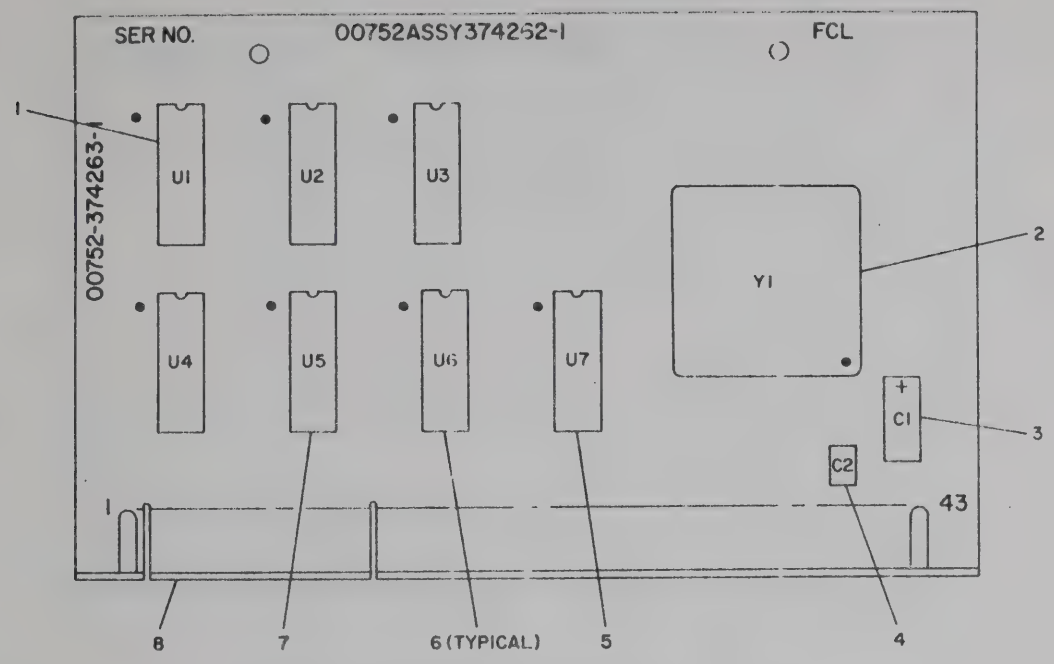


Figure 10. FCL Circuit Card Assembly (18A301)

FIG. AND INDEX NO.	PART NUMBER	1 2 3 4 5 6 7 DESCRIPTION	UNITS PER ASSY	USABLE ON CODE
10-	374262-1	CIRCUIT CARD ASSEMBLY (FCL) (18A301) (see fig 4-62 for nha)	Ref	
-1	373409-1	. INTEGRATED CIRCUIT	1	
-2	374186-7	. CRYSTAL OSCILLATOR	1	
-3	CSR13F685KL	. CAPACITOR	1	
-4	CK05BX103K	. CAPACITOR	1	
-5	373408-1	. INTEGRATED CIRCUIT	1	
-6	373401-1	. INTEGRATED CIRCUIT	4	
-7	373405-1	. INTEGRATED CIRCUIT	1	
-8	374263-1	. PRINTED CIRCUIT BOARD	1	

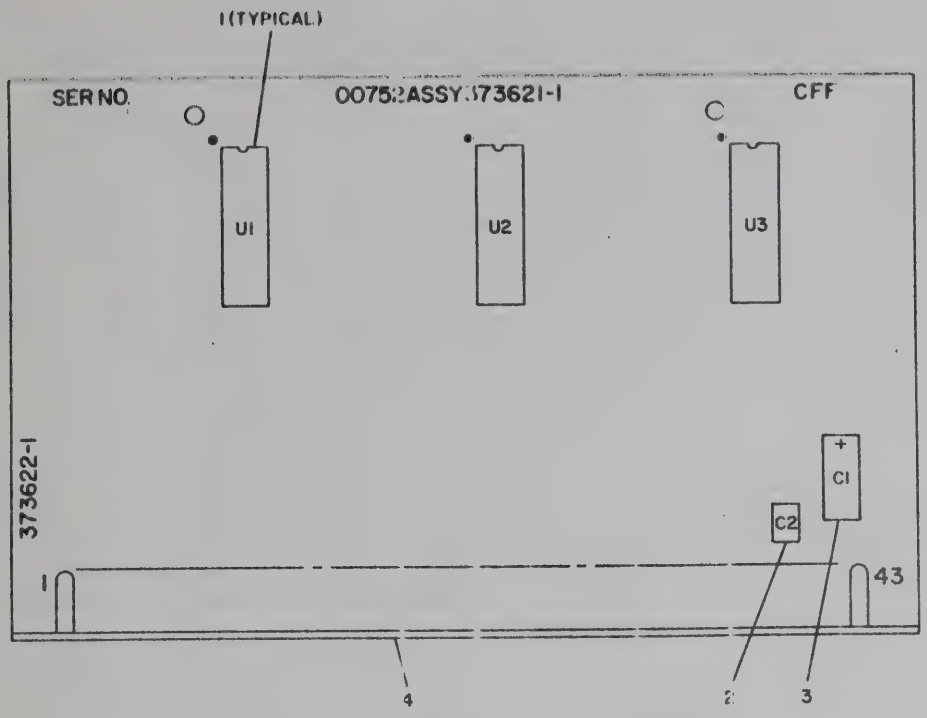


Figure 11. CFF Circuit Card Assembly

FIG. AND INDEX NO.	PART NUMBER	1 2 3 4 5 6 7 DESCRIPTION	UNITS PER ASSY	USABLE ON CODE
11-	373621-1	CIRCUIT CARD ASSEMBLY (CFF) (see fig 4-63 for nha)	Ref	
-1	373414-1	. INTEGRATED CIRCUIT	3	
-2	CK05BX103K	. CAPACITOR	1	
-3	CSR13F685KL	. CAPACITOR	1	
-4	373622-1	. PRINTED CIRCUIT BOARD	1	

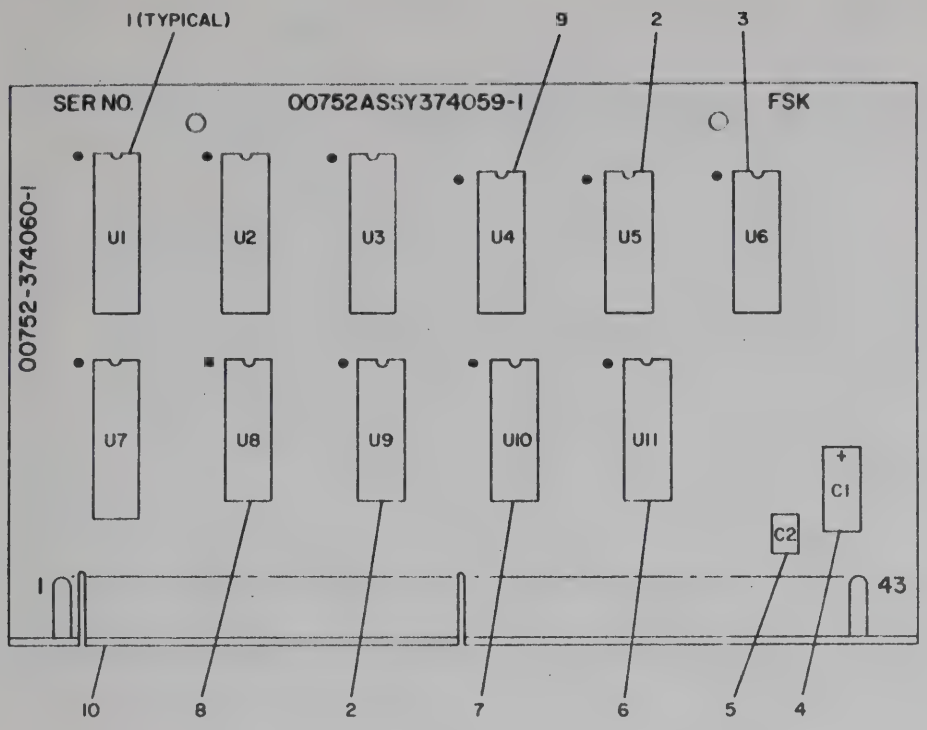


Figure 12. FSK Circuit Card Assembly

FIG. AND INDEX NO.	PART NUMBER	1 2 3 4 5 6 7 DESCRIPTION	UNITS PER ASSY	USABLE ON CODE
12-	374059-1	CIRCUIT CARD ASSEMBLY (FSK) (see fig 4-64 for nha)	Ref	
-1	373414-1	. INTEGRATED CIRCUIT	4	
-2	373409-1	. INTEGRATED CIRCUIT	2	
-3	373401-1	. INTEGRATED CIRCUIT	1	
-4	CSR13F685KL	. CAPACITOR	1	
-5	CK05BX103K	. CAPACITOR	1	
-6	373405-1	. INTEGRATED CIRCUIT	1	
-7	373404-1	. INTEGRATED CIRCUIT	1	
-8	373424-1	. INTEGRATED CIRCUIT	1	
-9	373427-1	. INTEGRATED CIRCUIT	1	
-10	374060-1	. PRINTED CIRCUIT BOARD	1	

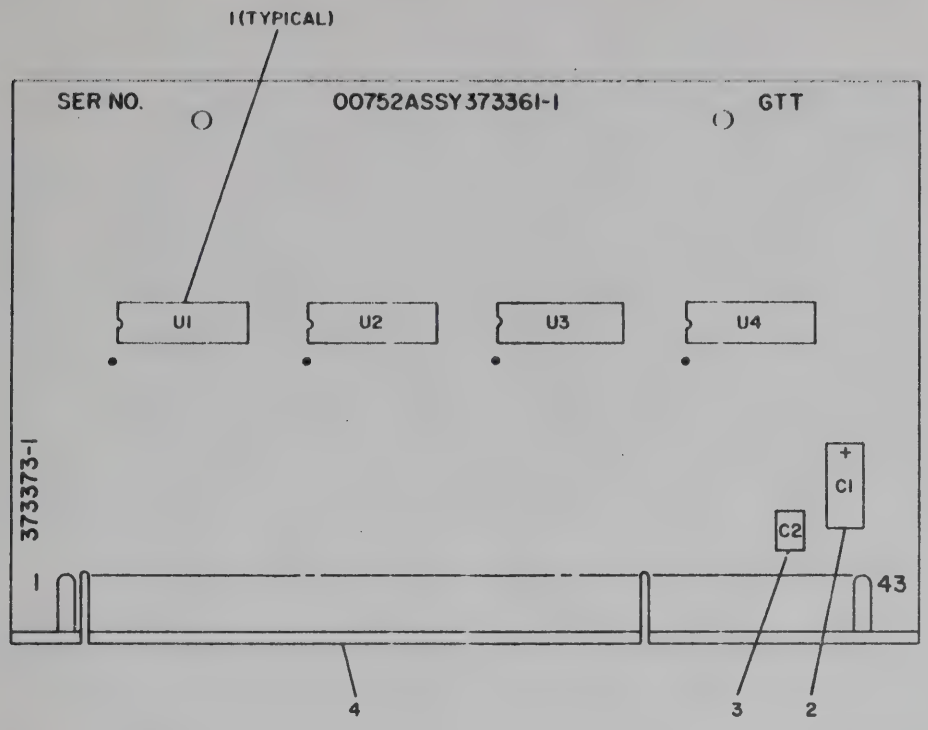


Figure 13. Two input (8) and 2 sets 4 two inputs GTT Circuit Card Assembly

FIG. AND INDEX NO.	PART NUMBER	1 2 3 4 5 6 7 DESCRIPTION	UNITS PER ASSY	USABLE ON CODE
13-	373361-1	CIRCUIT CARD ASSEMBLY (GTT) (see fig 4-65 for nha)	Ref	
-1	373401-1	. INTEGRATED CIRCUIT	4	
-2	CSR13F685KL	. CAPACITOR	1	
-3	CK05BX103K	. CAPACITOR	1	
-4	373373-1	. PRINTED CIRCUIT BOARD	1	

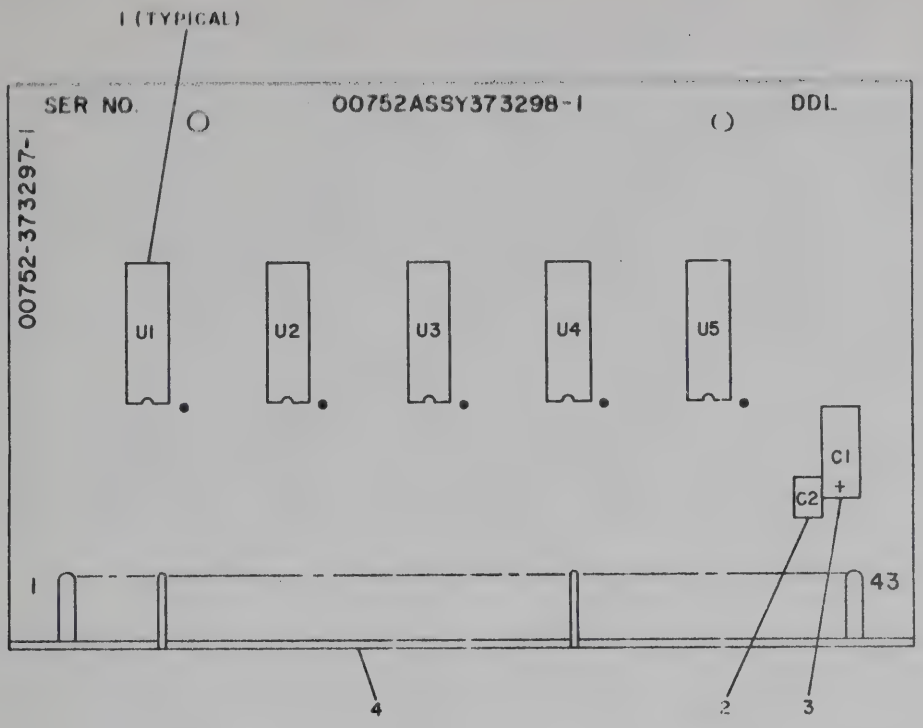


Figure 14. DDL Circuit Card Assembly

FIG. AND INDEX NO.	PART NUMBER	1 2 3 4 5 6 7 DESCRIPTION	UNITS PER ASSY	USABLE ON CODE
14-	373298-1	CIRCUIT CARD ASSEMBLY (DDL) (see fig 4-66 for nha)	Ref	
-1	373411-1	. INTEGRATED CIRCUIT	5	
-2	CSR13F685KL	. CAPACITOR	1	
-3	CK05BX103X	. CAPACITOR	1	
-4	373297-1	. PRINTED CIRCUIT BOARD	1	

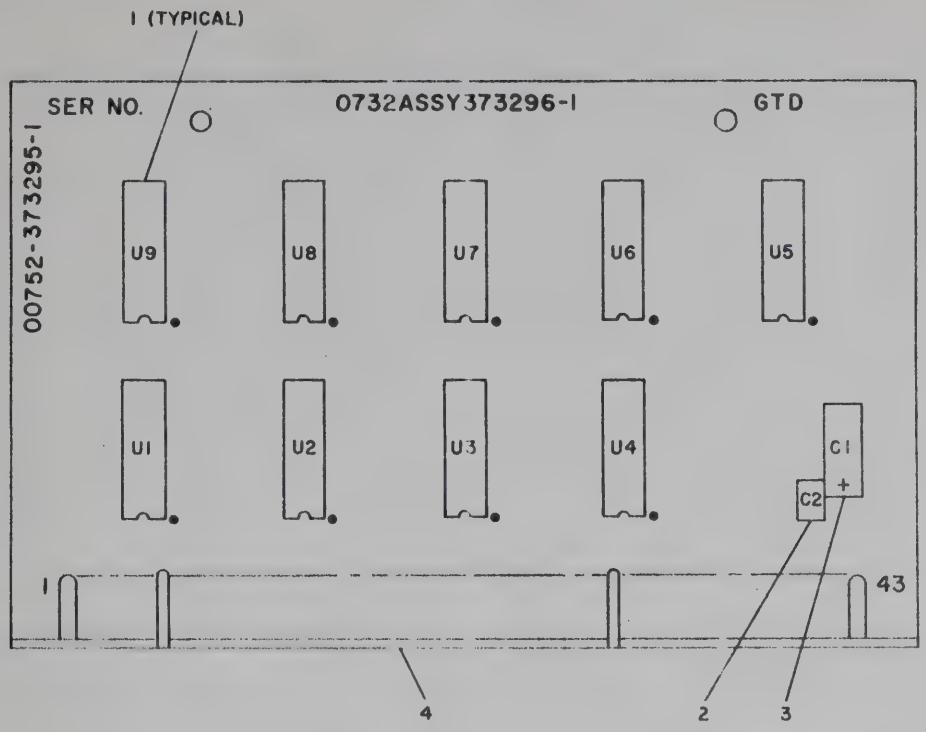


Figure 15. GTD Circuit Card Assembly

FIG. AND INDEX NO.	PART NUMBER	1 2 3 4 5 6 7 DESCRIPTION	UNITS PER ASSY	USABLE ON CODE
15-	373296-1	CIRCUIT CARD ASSEMBLY (GTD) (see fig 4-67 for nha)	Ref	
-1	373408-1	. INTEGRATED CIRCUIT	9	
-2	CK05BX103K	. CAPACITOR	1	
-3	CSR13F685KL	. CAPACITOR	1	
-4	373295-1	. PRINTED CIRCUIT BOARD	1	

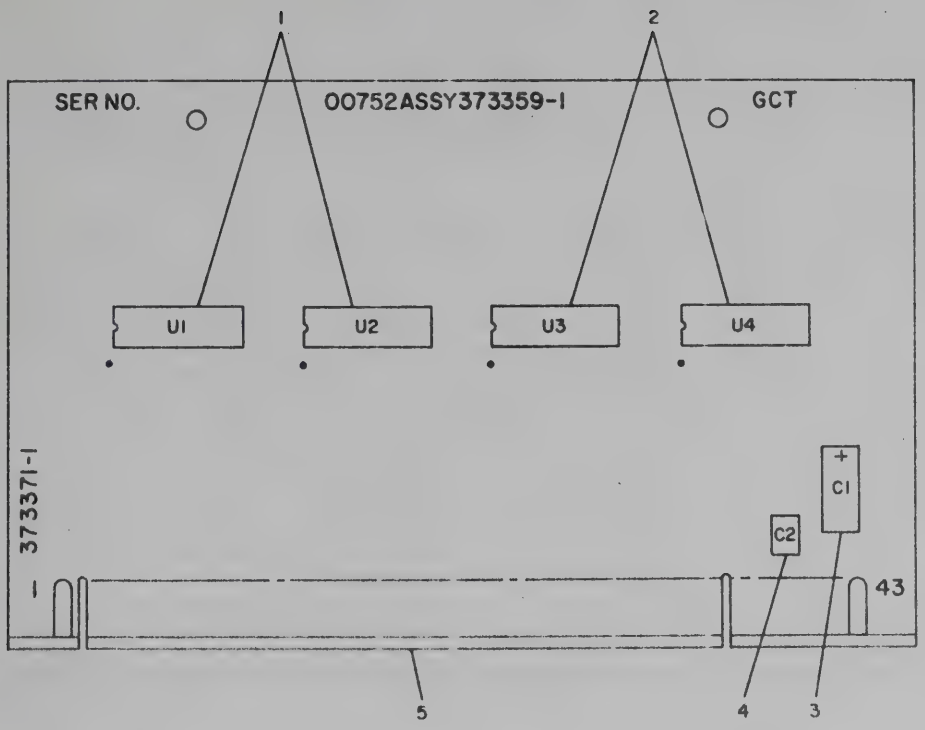


Figure 16. Four input (4) and eight input (2) GCT Circuit Card Assembly

FIG. AND INDEX NO.	PART NUMBER	1 2 3 4 5 6 7 DESCRIPTION	UNITS PER ASSY	USABLE ON CODE
16-	373359-1	CIRCUIT CARD ASSEMBLY (GCT) (see fig 4-68 for nha)	Ref	
-1	373406-1	. INTEGRATED CIRCUIT	2	
-2	373407-1	. INTEGRATED CIRCUIT	2	
-3	CSR13F685KL	. CAPACITOR	1	
-4	CK05BX103K	. CAPACITOR	1	
-5	373371-1	. PRINTED CIRCUIT BOARD	1	

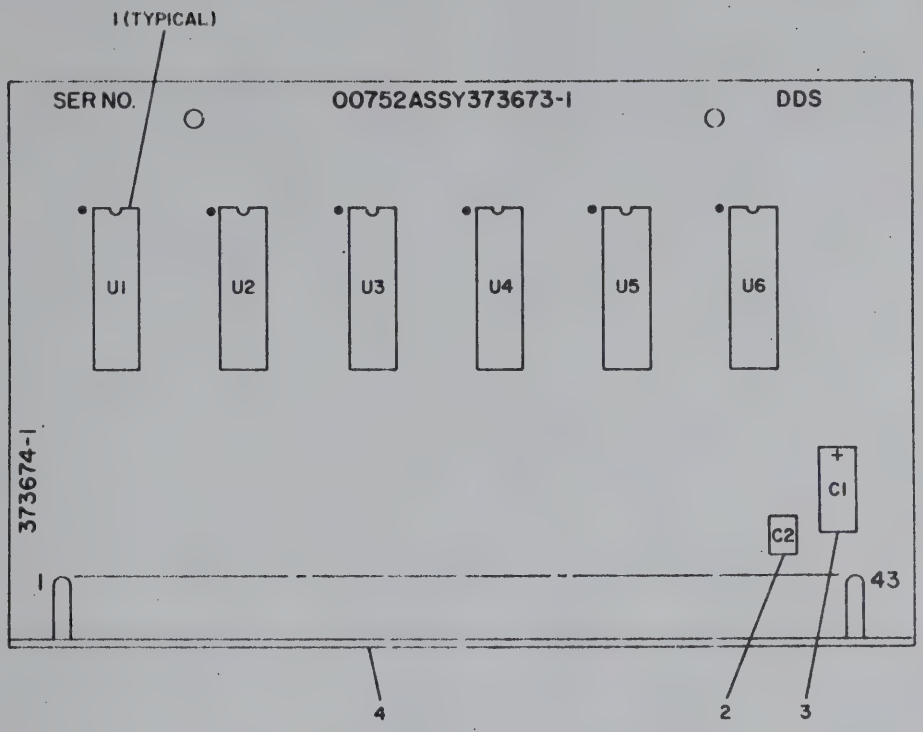


Figure 17. DDS Circuit Card Assembly

FIG. AND INDEX NO.	PART NUMBER	1 2 3 4 5 6 7 DESCRIPTION	UNITS PER ASSY	USABLE ON CODE
17-	373673-1	CIRCUIT CARD ASSEMBLY (DDS) (see fig 4-69 for nha)	Ref	
-1	373417-1	. INTEGRATED CIRCUIT	6	
-2	CK05BX103K	. CAPACITOR	1	
-3	CSR13F685KL	. CAPACITOR	1	
-4	373674-1	. PRINTED CIRCUIT BOARD	1	

SECTION III

NUMERICAL INDEX

PART NO.	FIG. AND INDEX NO.	QTY PER ART	SOURCE CODE	REPAIR CODE
AJ3-30SS	4-10	7	P1-	S
AJ3-35SS	4-52	7	P1-	S
CH53B1NF105M	9-4	1	P1-	S
CK05BX103K	10-4	38	P1-	S
	11-2			
	12-5			
	13-3			
	14-3			
	15-2			
	16-4			
	17-2			
CSR13F685KL	10-3	38	P1-	S
	11-3			
	12-4			
	13-2			
	14-2			
	15-3			
	16-3			
	17-3			
D9597-1	1-5	1	X2-	S
FHN26G	5-12	2	P1-	S
F02A125V3AS	5-11	1	P1-	S
GR100MISLWWP	4-44	4	P1-	S
JAN1N4148	6-1	69	P1-	S
	7-1			
	8-1			
LC13WT2	5-7	1	P1-	S
LH74-1	5-9	1	P1-	S
MS15795-803	4-	143	P1-	S
MS15795-805	4-	30	P1-	S
MS15795-807	4-	2	P1-	S
MS24655-231	5-33	8	P1-	S
MS24656-231	4-20	1	P1-	S
MS24693C51	5-	4	P1-	S
MS25089-3C	5-14	5	P1-	S
MS25252C7A	5-8	1	P1-	S
MS3122E14-5P	5-6	1	P1-	S
MS3124E20-41P	5-15	1	P1-	S
MS3124E14-5P	4-21	1	P1-	S
MS3124E22-55P	5-16	1	P1-	S
MS3126F14-5S	3-1	1	P1-	S
MS3126F18-11S	3-1	1	P1-	S
MS3126F20-41P	3-3	1	P1-	S
MS3126F20-41S	3-1	1	P1-	S
MS3126F22-55P	3-3	1	P1-	S
MS3126F22-55S	3-1	1	P1-	S
MS35059-23	5-10	1	P1-	S
MS35338-135	4-	117	P1-	S
MS35338-136	4-	10	P1-	S
MS35338-137	9-8	1	P1-	S
MS35338-138	9-3	6	P1-	S
MS35489-4	4-53	2	P1-	S
MS35649-244	4-	94	P1-	S
MS35649-264	4-	8	P1-	S
MS35649-284	9-9	1	P1-	S
MS51957-1	4-	1	P1-	S
MS51957-14	4-28	21	P1-	S
MS51957-15	4-	8	P1-	S
MS51957-16	4-	21	P1-	S
MS51957-17	4-	10	P1-	S
MS51957-30	4-23	22	P1-	S
MS51957-37	4-	1	P1-	S
MS51957-126	4-4	2	P1-	S
MS51958-64	9-2	6	P1-	S
MS51958-92	4-7	2	P1-	S
MS51959-14	9-29	4	P1-	S
MS51959-16	4-	9	P1-	S
MS51959-261	5-	1	P1-	S
MS51959-32	9-21	3	P1-	S
MS51959-45	9-6	1	P1-	S
M39012-21-003	5-13	4	P1-	S
PT05NC01	5-4	1	X2-	S
RCR05G301JS	5-2	69	P1-	S
SFSW8C8D-S01BK	4-3	9	X2-	S
UP221M	3-3	1	P1-	S
1038-1	5-28	2	X2-	S
1039-1	9-10	1	X2-	S
10382DAP	6-4	69	P1-	S
	7-3			
	8-3			
1733	1-3	1	P1-	S
1941-2-01	6-4	102	P1-	S
	7-4			
	8-4			
3SS	4-9	14	P1	S
	4-51			
317841-1	4-8	1	P1-	S
33003-714	4-60	1	P1	S
370782-3	4-	1	P1-	S
371132-1	4-18	1	X2-	S
371693-3	5-5	1	X2-	S
371956-1	4-16	1	P1-	S
372215-1	4-46	42	P1-	S
373295-1	10-4	18	X1	
373296-1	4-67	18	P1	D
373297-1	11-4	3	X1	
373298-1	4-66	3	P1	D
373350-1	9-1	1	P1	D
373359-1	4-68	2	P1	D
373361-1	4-65	4	P1	D
373371-1	16-5	1	X1	
373373-1	13-4	4	X1	
373401-1	10-6	21	P1-	S
	12-3			
	13-1			
373404-1	12-7	1	P1-	S
373405-1	10-7	2	P1-	S
	12-6			
373406-1	16-1	4	P1-	S
373407-1	16-2	4	P1-	S
373408-1	10-5	16	P1-	S
	14-1			
373409-1	10-1	3	P1-	S
	12-2			
373411-1	14-1	15	P1-	S
373414-1	11-1	13	P1-	S
	12-1			
373417-1	17-1	36	P1-	S
373424-1	12-8	1	P1-	S
373427-1	12-9	1	P1-	S
373621-1	4-63	3	P1	D
373622-1	11-4	3	X1	
373673-1	4-69	6	P1	D
	17-			
373674-1	17-4	6	X1-	
373868-1	4-35	3	X2-	S
374059-1	4-64	1	P1-	D
374060-1	12-10	1	X1-	
374117-3	4-58	1	P1-	S
374118-1	4-45	88	X2-	S
374186-7	10-2	1	P1-	S
374262-1	4-62	1	P1	D
374263-1	10-8	1	X1-	
374671-1	1-	1	P1	D
374654-1 (see pn SFSW8C8DS01BK)				
374654-7	5-	32	X2-	S
374655-1	5-	8	P1-	S
374656-1	5-	8	P1-	S
374694-3 (see pn GR100MISLWWP)				
385055-1	4-54	1	P1-	S
385056-3	4-55	4	P1-	S
385546-1 (see pn 1733)				
385595-1	6-3	69	P1-	S
	7-3			
	8-3			
385598-1	4-17	4	X1-	
385682-1	6-8	3	X1-	
	7-5			
	8-5			
385683-1	5-20	7	P1	D
	6			
385907-1 (see pn 10382DAP)				
385908-1 (see pn 7717-149DAP)				
385944-1 (see pn 919B1900A)				
385987-1	4-70	1	X2-	S
385992-1	5-21	1	P1	D
	7-			
385995-1	5-22	1	P1-	D
	8-			
386002-1	4-	1	X2-	S
386003-1	4-61	1	X2-	S
386004-1	4-59	1	X2-	S
386005-1	5-34	1	X2-	S
386021-1	4-2	1	X2-	S
386030-1	4-25	1	X2-	S

Change 1

PART NO.	FIG. AND INDEX NO.	QTY PER ART	SOURCE CODE	REPAIR CODE
386040-1	5-1	2	P1-	S
386041-1	1-45	1	X1	
386045-1	5-2	1	X2-	
386055-1	4-47	1	P1-	S
386056-1	4-	1	X1	
386090-1	4-	1	AF	
386105-1	4-19	1	X2-	S
386106-1	4-	1	P1-	S
386114-2	4-11	1	X2-	S
386115-1	4-	1	X2-	S
386116-1	5-3	1	X2-	
386131-1	4-36	1	X2-	S
386132-1	4-38	2	X2-	S
386133-1	4-37	1	X2-	S
386134-1	4-39	1	X2-	S
386135-1	4-40	1	X2-	S
386136-1	4-	1	X2-	S
386137-1	9-21	1	X2-	S
386250-1	4-43	4	X2-	F
386260-1	4 26	2	X2-	S
386507-1 (see pn 09597-1)				
386576-1	5-	4	X2-	S
386614-1	9-25	1	MF-	S
387015-1	4-5	1	X2-	S
387076-1	4-22	1	AF-	
387165-1	1-2	1	MF-	
	2-			
387167-1	1-3	1	MF-	
	3-			
387168-1	1-3	1	MF-	
	3-			
387169-1	1-3	1	MF-	
	3-			
387170-1	1-3	1	MF-	
	3-			
387182-1	4-6	2	X2-	S
387342-1	2 2	1	X2-	S
386268-1	5-27	54	P1-	S
387342-3	3-2	1	X2-	S
387342-4	3-2	1	X2-	S
387342-5	3-2	1	X2-	S
387342-6	3-2	1	X2-	S
387358-1 (see pn 1941-2-01)				
387459-1	1-1	2		
387585-1	1-	1		
626-4	5-17	1	X2-	S
7717-149DAP	7-3	69	P1-	S
	6-5			
	8-3			
8TB10	9-20	1	P1-	S
805-4	9-15	1	X2-	S
805-8	9-5	1	X2-	S
919B1900A	2-1	1	P1-	S
972-301	5-26	54	P1	S
974-302	5-32	2	P1-	S
990031 42	9-28	4	X2-	S

SECTION IV

REFERENCE DESIGNATION INDEX

REFERENCE DESIGNATION	FIG. AND INDEX NO.	PART NUMBER
18-	1-	374571-1
18A1	5-20	385883-1
18A1CR1 thru 18A1CR32	6-1	JAN1N4148
18A1DS1 thru 18A1DS32	6-3	385595-1
18A1R1 thru 18A1R32	6-2	RCR05G301JS
18A10	4-	386090-1
18A10J2 thru 18A10J5	4-44	GR100MISLWWP
18A102	4-67	373296-1
18A102C1	15-3	CSR13F685KL
18A102C2	15-2	CK05BX103K
18A102U1 thru 18A102U9	15-1	373408-1
18A103	4-67	373296-1
18A103C1	15-3	CSR13F685KL
18A103C2	15-2	CK05BX103K
18A103U1 thru 18A103U9	15-1	373408-1
18A104	4-67	373296-1
18A104C1	15-3	CSR13F685KL
18A104C2	15-2	CK05BX103K
18A104U1 thru 18A104U9	15-1	373408-1
18A105	4-67	373296-1
18A105C1	15-3	CSR13F685K1
18A105C2	15-2	CK05BX103K
18A105U1 thru 18A105U9	15-1	373408-1
18A106	4-67	373296-1
18A106C1	15-3	CSR13F685KL
18A106C2	15-2	CK05BX103K
18A106U1 thru 18A106U9	15-1	373408-1
18A107	4-67	373296-1
18A107C1	15-3	CSR13F685KL
18A107C2	15-2	CK05BX103K
18A107U1 thru 18A107U9	15-1	373408-1
18A108	4-66	373298-1
18A108C1	14-2	CSR13F685KL
18A108C2	14-3	CK05BX103X
18A108U1 thru 18A108U5	14-1	373411-1
18A109	4-67	373296-1
18A109C1	15-3	CSR13F685KL
18A109C2	15-2	CK05BX103K
18A109U1 thru 18A109U9	15-1	373408-1
18A11	4-22	387076-1
18A11C1	9-4	CH53B1NF105M
18A11E1	9-5	990209-3
18A11E2	9-10	990313-1
18A11E3	9-15	990209-1
18A11PS1	9-1	373350-1
18A11TB1	9-20	8TB10
18A110	4-69	373673-1
18A11C1	17-3	CSR13F685KL
18A110C2	17-2	CK05BX103K
18A110U1 thru 18A110U6	17-1	373417-1
18A111	4-67	373296-1
18A111C1	15-3	CSR13F685KL
18A111C2	15-2	CK05BX103K
18A111U1 thru 18A111U9	15-1	373408-1
18A112	4-67	373296-1
18A112C1	15-3	CSR13F685KL
18A112C2	15-2	CK05BX103K
18A112U1 thru 18A112U9	15-1	373408-1
18A113	4-69	373673-1
18A113C1	17-3	CSR13F685KL
18A113C2	17-2	CK05BX103K
18A113U1 thru 18A113U6	17-1	373417-1
18A114	4-69	373673-1
18A114C1	17-3	CSR13F685KL
18A114C2	17-2	CK05BX103K
18A114U1 thru 18A114U6	17-1	373417-1
18A2	5-20	385883-1
18A2CR1 thru 18A2CR32	6-1	JAN1N4148
18A2DS1 thru 18A2DS32	6-3	385595-1
18A2R1 thru 18A2R32	6-2	RCR05G301JS
18A202	4-65	373661-1
18A202C1	13-2	CSR13F685KL
18A202C2	13-3	CK05BX103K
18A202U1 thru 18A202U4	13-1	373401-1
18A203	4-67	373296-1
18A203C1	15-3	CSR13F685KL
18A203C2	15-2	CK05BX103K
18A203U1 thru 18A203U9	15-1	373408-1
18A204	4-65	373661-1
18A204C1	13-2	CSR13F685KL
18A204C2	13-3	CK05BX103K
18A204U1 thru 18A204U4	13-1	373401-1
18A205	4-67	373296-1
18A205C1	15-3	CSR13F685KL
18A205C2	15-2	CK05BX103K
18A205U1 thru 18A205U9	15-1	373408-1
18A206	4-67	373296-1
18A206C1	15-3	CSR13F685KL
18A206C2	15-2	CK05BX103K
18A206U1 thru 18A206U9	15-1	373408-1
18A207	4-67	373296-1
18A207C1	15-	373296-1
18A207C1	15-3	CSR13F685KL
18A207C2	15-2	CK05BX103K
18A207U1 thru 18A207U9	15-1	373408-1
18A208	4-66	373298-1
18A208C1	14-2	CSR13F685KL
18A208C2	14-3	CK05BX103Y
18A208U1 thru 18A208U5	14-1	373411-1
18A209	4-67	373296-1
18A209C1	15-3	CSR13F685KL
18A209C2	15-2	CK05BX103K
18A209U1 thru 18A209U9	15-1	373408-1
18A210	4-69	373673-1
18A210C1	17-3	CSR13F685KL
18A210C2	17-2	CK05BX103K
18A210U1 thru 18A210U6	17-1	373417-1
18A211	4-67	373296-1
18A211C1	15-3	CSR13F685KL
18A211C2	15-2	CK05BX103K
18A211U1 thru 18A211U9	15-1	373408-1
18A212	4-67	373296-1

REFERENCE DESIGNATION	FIG. AND INDEX NO.	PART NUMBER
18A212C1	15-3	CSR13F685KL
18A212C2	15-2	CK05BX103K
18A212U1 thru 18A212U9	15-1	373408-1
18A213	4-67	373296-1
18A213C1	15-3	CSR13F685KL
18A213U1 thru 18A213U9	15-1	373408-1
18A213C2	15-2	CK05BX103K
18A3	5-21	385992-1
18A3CR1 thru 18A3CR17, 18A3CR19, 18A3CR21, 18A3CR23, 18A3CR25, 18A3CR26, 18A3CR27, 18A3CR29, 18A3CR31	7-1	JAN1N4148
18A3DS1 thru 18A3DS17, 18A3DS19, 18A3DS21, 18A3DS23, 18A3DS25, 18A3DS26, 18A3DS27, 18A3DS29, 18A3DS31	7-3	385595-1
18A3R1 thru 18A3R17, 18A3R19, 18A3R21, 18A3R23, 18A3R25, 18A3R26, 18A3R27, 18A3R29, 18A3R31	7-2	RCR05G301JS
18A301	4-62	374262-1
18A301C1	10-3	CSR13F685KL
18A301C2	10-4	CK05BX103K
18A301U1	10-1	373409-1
18A301U2 thru 18A301U4	10-6	373401-1
18A301U5	10-7	373405-1
18A301U6	10-6	373401-1
18A301U7	10-5	373408-1
18A301P1	10-2	374186-7
18A303	4-63	373621-1
18A303C1	11-3	CSR13F685KL
18A303C2	11-2	CK05BX103K
18A303U1 thru 18A303U3	11-1	373414-1
18A304	4-63	373621-1
18A304C1	11-3	CSR13F685KL
18A304C2	11-2	CK05BX103K
18A304U1 thru 18A304U3	11-1	373414-1
18A305	4-64	374059-1
18A305C1	12-4	CSR13F685KL
18A305C2	12-5	CK05BX103K
18A305U1 thru 18A305U3	12-1	373414-1
18A305U4	12-9	373527-1
18A305U5	12-2	373409-1
18A305U6	12-3	373401-1
18A305U7	12-1	373414-1
18A305U8	12-8	373424-1
18A305U9	12-2	373409-1
18A305U10	12-7	373404-1
18A305U11	12-6	373405-1
18A306	4-65	373361-1
18A306C1	13-2	CSR13F685KL
18A306C2	13-3	CK05BX103K
18A306U1 thru 18A306U4	13-1	373401-1
18A307	4-65	373361-1
18A307C1	13-2	CSR13F685KL
18A307C2	13-3	CK05BX103K
18A307U1 thru 18A307U4	13-1	373401-1
18A308	4-66	373298-1
18A308C1	14-2	CSR13685KL
18A308C2	14-3	CK05BX103X
18A308U1 thru 18A308U5	14-1	373411-1
18A309	4-63	373621-1
18A309C1	11-3	CSR13F685KL
18A309C2	11-2	CK05BX103K
18A309U1 thru 18A309U3	11-1	373414-1
18A310	4-67	373296-1
18A310C1	15-3	CSR13F685KL
18A310C2	15-2	CK05BX103K
18A310U1 thru 18A310U9	15-1	373408-1

REFERENCE DESIGNATION	FIG. AND INDEX NO.	PART NUMBER
18A311	4-68	373359-1
18A311C1	16-3	CSR13F685KL
18A311C2	16-4	CK05BX103K
18A311U1, 18A311U2	16-1	373406-1
18A311U3, 18A311U4	16-2	373407-1
18A312	4-68	373359-1
18A312C1	16-3	CSR13F685KL
18A312C2	16-4	CK05BX103K
18A312U1, 18A312U2	16-1	373406-1
18A312U3, 18A312U4	16-2	373407-1
18A313	4-69	373673-1
18A313C1	17-3	CSR13F685KL
18A313C2	17-2	CK05BX103K
18A313U1 thru 18A313U6	17-1	373417-1
18A314	4-69	373673-1
18A314C1	17-3	CSR13F685KL
18A314C2	17-2	CK05BX103K
18A314U1 thru 18A314U6	17-1	373417-1
18A4	5-20	385583-1
18A4CR1 thru 18A4CR32	6-1	JAN1N4148
18A4DS1 thru 18A4DS32	6-3	385595-1
18A4R1 thru 18A4R32	6-2	RCR05G301JS
18A5	5-20	385883-1
18A5CR1 thru 18A5CR32	6-1	JAN1N4148
18A5DS1 thru 18A5DS32	6-3	385595-1
18A5R1 thru 18A5R32	6-2	RCR05G301JS
18A6	5-20	385583-1
18A6CR1 thru 18A6CR32	6-1	JAN1N4148
18A6DS1 thru 18A6DS32	6-3	385595-1
18A6R1 thru 18A6R32	6-2	RCR05G301JS
18A7	5-20	385883-1
18A7CR1 thru 18A7CR32	6-1	JAN1N4148
18A7DS1 thru 18A7DS32	6-3	385595-1
18A7R1 thru 18A7R32	6-2	RCR05G301JS
18A8	5-22	385995-1
18A8CR6, 18A8CR8, 18A8CR10, 18A8CR12, 18A8CR14, 18A8CR16, 18A8CR18, 18A8CR20, 18A8CR22, 18A8CR24, 18A8CR26, 18A8CR28	8-1	JAN1N4148
18A8DS6, 18A8DS8, 18A8DS12, 18A8DS14, 18A8DS16, 18A8DS18, 18A8DS20, 18A8DS22, 18A8DS24, 18A8DS26, 18A8DS28	8-3	385595-1
18A8R6, 18A8R8, 18A8R10, 18A8R12, 18A8R14, 18A8R16, 18A8R18, 18A8R20, 18A8R22, 18A8R24, 18A8R26, 18A8R28	8-2	RCR05G301JS
18A9	5-20	385883-1
18A9CR1 thru 18A9CR32	6-1	JAN1N4148
18A9DS1 thru 18A9DS32	6-3	385595-1
18A9R1 thru 18A9R32	6-2	RCR05G301JS
18DS1	5-8	MS25252C7A
18E1	5-17	990205-1
18E2, 18E3	5-28	990313-2
18FL1	4-	386106-1
18FL1E1	4-16	371956-1
18FL1FL2 thru 18FL1FL4	4-17	385598-1
18F1, 18F2	5-11	F02A125V3AS
18J1	5-6	MS3122E14-5P
18J2 thru 18J5	5-13	M39012/21-003
18J6	5-15	MS3124E20-41P
18J7	5-16	MS3124E22-55P
18J8	4-21	MS3124E14-5P
18S1	5-10	MS35059-23
18S13	5-14	MS25089-3C
18S14	4-20	MS24656-231
18S15	5-14	MS25089-3C

REFERENCE DESIGNATION	FIG. AND INDEX NO.	PART NUMBER
18J2 thru 18J4	5-14	MS25089 3C
18J5 thru 18J12	5-33	MS24655 231
18XA101 thru 18XA114	4-46	372215 1

REFERENCE DESIGNATION	FIG. AND INDEX NO.	PART NUMBER
18XA204 thru 18XA214	4-46	372215 1
18XA301 thru 18XA314	4-46	372215 1
18XF1, 18XF2	5-12	FHN26G

(USAF) T.O. 33D7-24-13-3

PRELIMINARY TECHNICAL MANUAL

CIRCUIT DIAGRAMS

TEST SET, VIDEO SIGNAL PROCESSOR MODEL AN/TPM-32

(AIRBORNE INSTRUMENTS LABORATORY
DIVISION OF CUTLER-HAMMER INC)

F33657-70-C-0207

PUBLISHED UNDER AUTHORITY OF THE SECRETARY
OF THE AIR FORCE AND BY DIRECTION OF THE
CHIEF OF THE NAVAL AIR SYSTEMS COMMAND

15 NOVEMBER 1971

Reproduction for nonmilitary use of the information or illustrations contained in this publication is not permitted without specific approval of the issuing service. The policy for use of Classified Publications is established for the Air Force in AFR 205-1.

Technical orders are normally distributed promptly after printing. Date(s) shown on the title page (lower right corner) are for identification only. This is not a distribution date. Processing time sometimes causes distribution to only appear to have been delayed.

LIST OF EFFECTIVE PAGES

INSERT LATEST CHANGED PAGES. DESTROY SUPERSEDED PAGES.

NOTE: The portion of the text affected by the changes is indicated by a vertical line in the outer margins of the page. Changes to illustrations are indicated by miniature pointing hands. Changes to wiring diagrams are indicated by shaded areas.

Dates of issue for original and changed pages are:
Original. 0

TOTAL NUMBER OF PAGES IN THIS PUBLICATION IS 26 CONSISTING OF THE FOLLOWING:

Page No.	*Change No.*
Title	0
A	0
i thru iii	0
1 thru 22	0

Upon receipt of the second and subsequent changes to this technical order, personnel responsible for maintaining this publication in current status will ascertain that all previous changes have been received and incorporated. Action should be taken promptly if the publication is incomplete.

* The asterisk indicates pages changed, added or deleted by the current change.

ADDITIONAL COPIES OF THIS PUBLICATION MAY BE OBTAINED BY USAF ACTIVITIES IN ACCORDANCE WITH T.O. 00-5-2

USAF

TABLE OF CONTENTS

Figure		Page
Introduction		ii
	SCHEMATIC WIRING DIAGRAM	
1	Video Signal Processor Test Set, Schematic Wiring Diagram	1
	OVERALL LOGIC DIAGRAM	
2	Video Signal Processor Test Set, Overall Logic Diagram	4
	CIRCUIT CARD SCHEMATICS	
3	GTT, Circuit Card Schematic	15
4	GTD, Circuit Card Schematic	16
5	GCT, Circuit Card Schematic	17
66	FCL, Circuit Card Schematic	18
7	FSK, Circuit Card Schematic	19
8	DDS, Circuit Card Schematic	20
9	DDL, Circuit Card Schematic	21
10	CFF, Circuit Card Schematic	22

INTRODUCTION

PURPOSE. This technical manual illustrates, by schematic and schematic wiring diagrams, all circuits and interconnections of the Test Set, Video Signal Processor AN/TPM-32 (hereafter referred to as test set).

SCOPE. This manual provides the following types of circuit diagrams: schematic wiring diagrams, overall logic diagram, and circuit card schematic diagrams.

SCHEMATIC WIRING DIAGRAMS. Basically, the schematic wiring diagrams are schematic diagrams which show all interconnections between the assemblies of the test set. Color codes of the interconnecting wires are also included.

OVERALL LOGIC DIAGRAM. The overall logic diagram shows timing and functional relationships between assemblies of the test set.

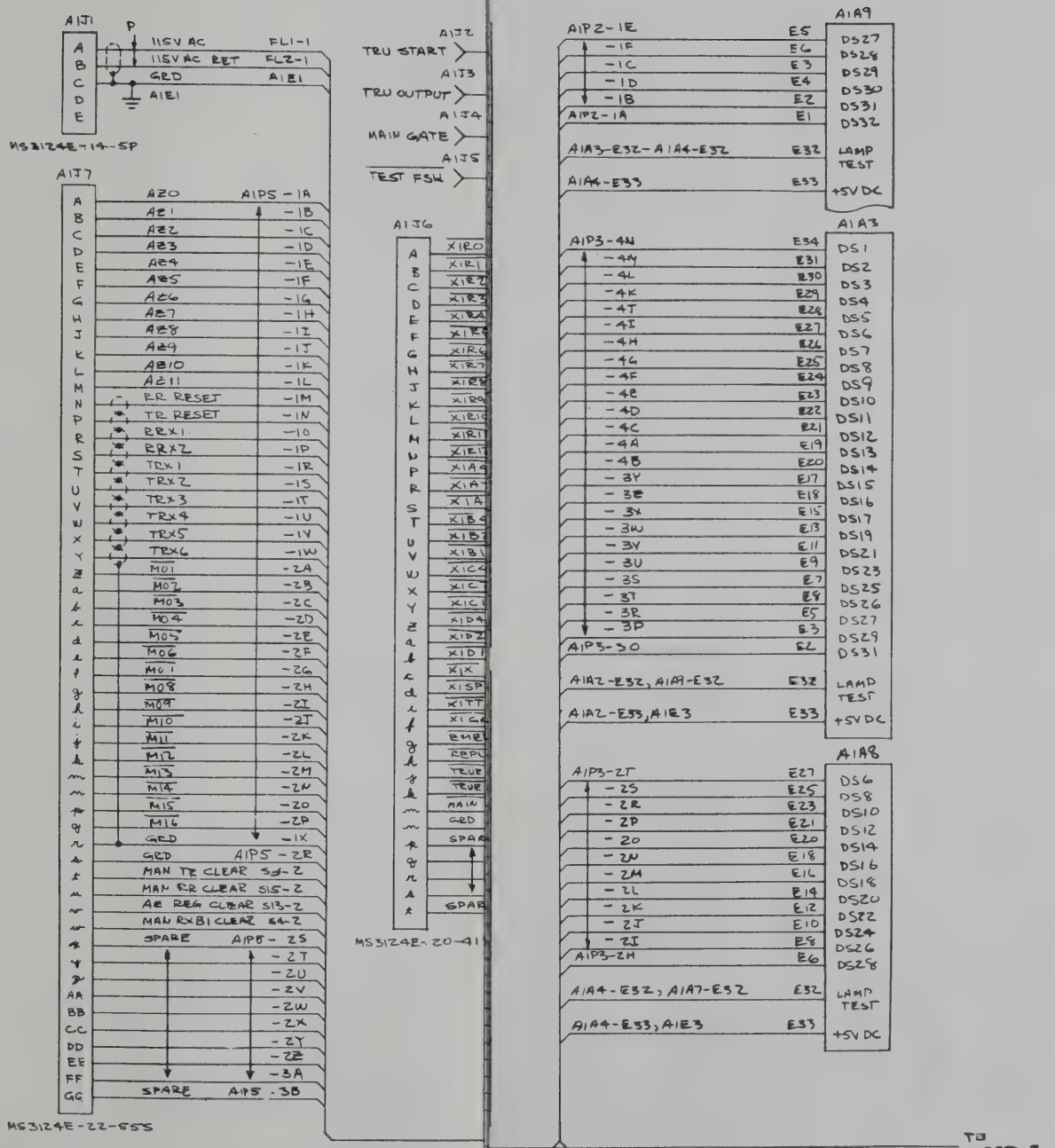
CIRCUIT CARD SCHEMATICS. The circuit card schematic diagrams show detailed circuitry of each circuit card assembly within the test set.

CIRCUIT DIAGRAM REFERENCE DATA. All graphic, electrical and electronic symbols conform with Specification MIL-STD-15. All abbreviations used in this manual conform with Specification MIL-STD-12.

The following statements are applicable to circuit diagrams contained in this manual.

a. Unless otherwise indicated, all resistance values are in ohms, and all capacitance values in microfarads.

b. All switches are viewed from the front unless otherwise noted.



A61087-1-1

FIGURE 1. VIDEO SIGNAL PROCESSOR TEST SET SCHEMATIC WIRING DIAGRAM (SHEET 1 OF 3)

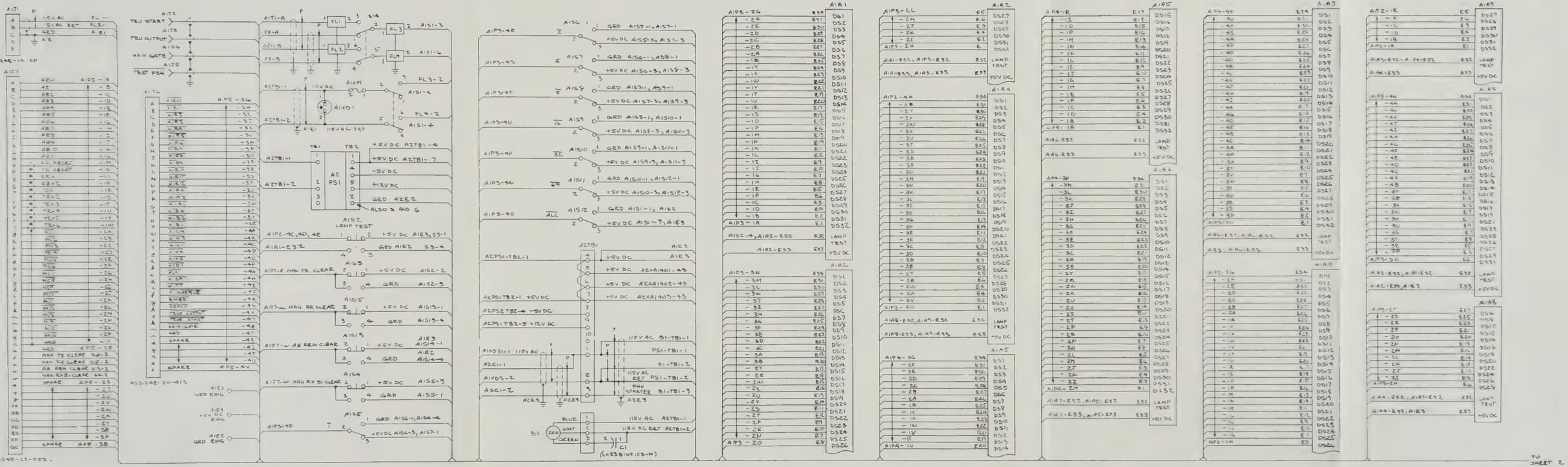
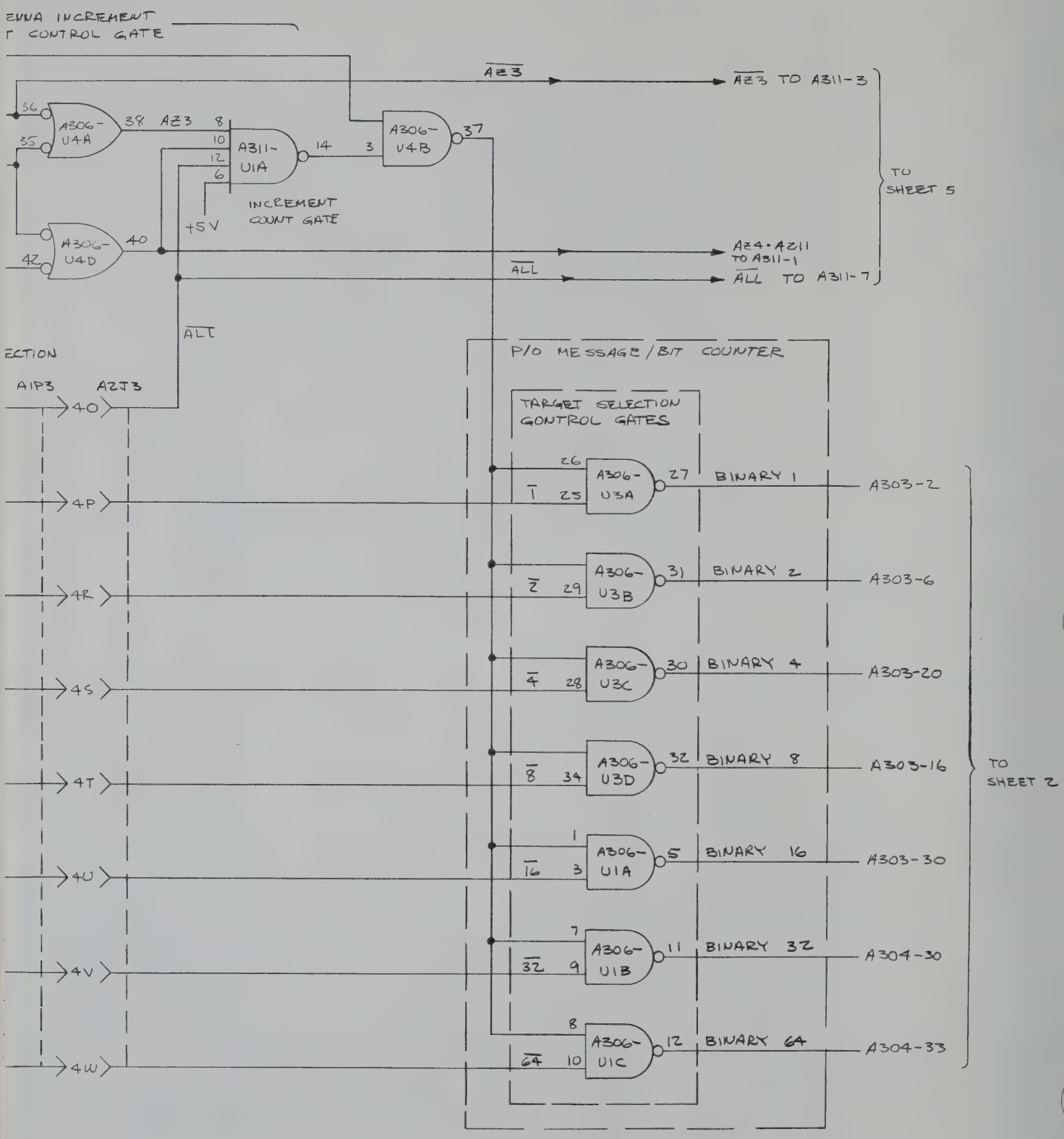


FIGURE 1. VIDEO SIGNAL PROCESSOR TEST SET SCHEMATIC WIRING DIAGRAM (SHEET 1 OF 3)


EVNA INCREMENT
T CONTROL GATE
AZ3
AZ3 TO A311-3
TO SHEET 5
A306-U4A
A311-U1A
A306-U4B
INCREMENT COUNT GATE
+5V
A306-U4D
AZ4·AZ11 TO A311-1
ALL
ALL TO A311-7
ALT
ECTION
P/O MESSAGE/BIT COUNTER
AIP3
AZT3
TARGET SELECTION CONTROL GATES
4O
4P
4R
4S
4T
4U
4V
4W
A306-U3A
A306-U3B
A306-U3C
A306-U3D
A306-U1A
A306-U1B
A306-U1C
BINARY 1
BINARY 2
BINARY 4
BINARY 8
BINARY 16
BINARY 32
BINARY 64
A303-2
A303-6
A303-20
A303-16
A303-30
A304-30
A304-33
TO SHEET 2

A61037-2-1

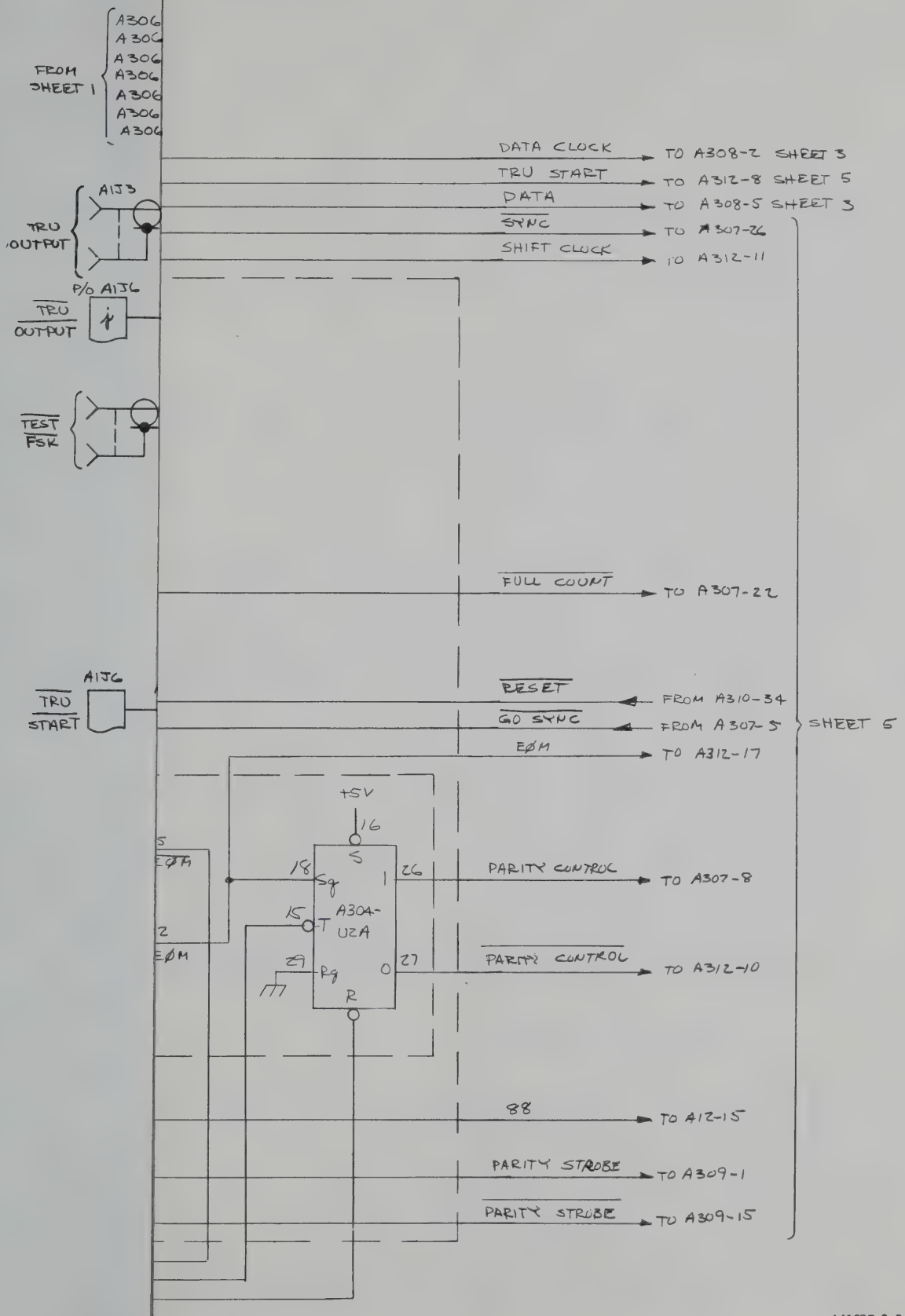


FIGURE 2. VIDEO SIGNAL PROCESSOR TEST SET OVERALL LOGIC DIAGRAM (SHEET 2 OF 11)

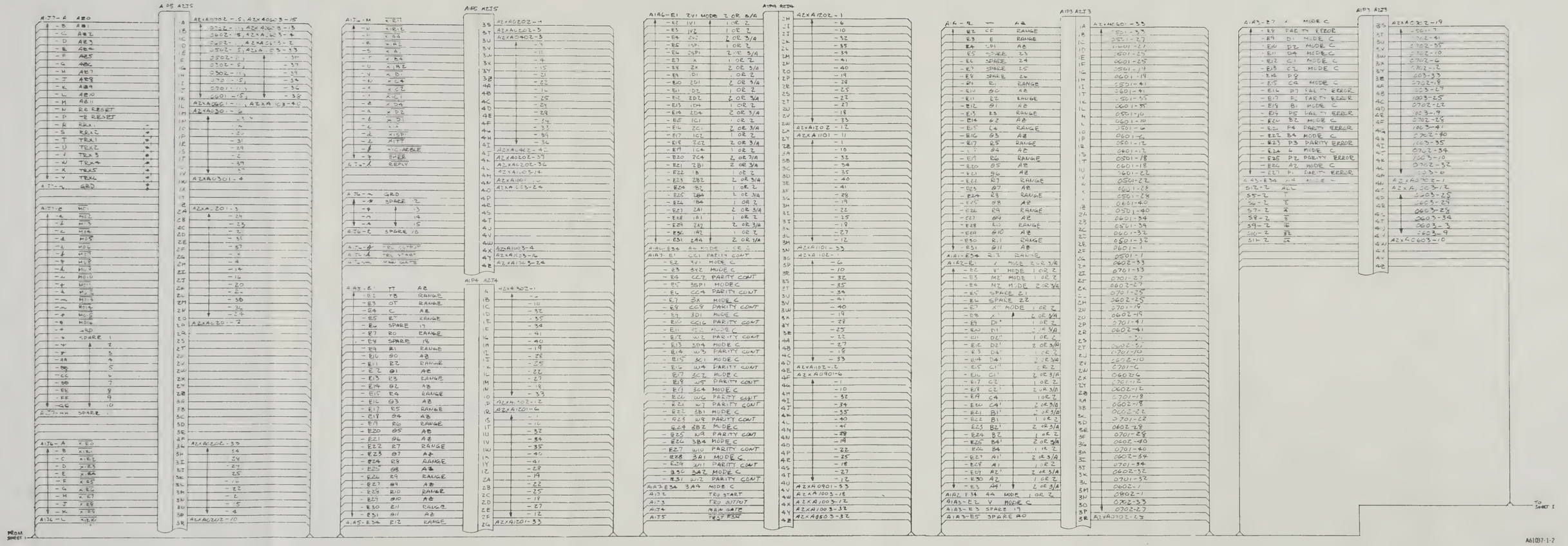


FIGURE 1. VIDEO SIGNAL PROCESSOR TEST SET SCHEMATIC WIRING DIAGRAM (SHEET 2 OF 3)

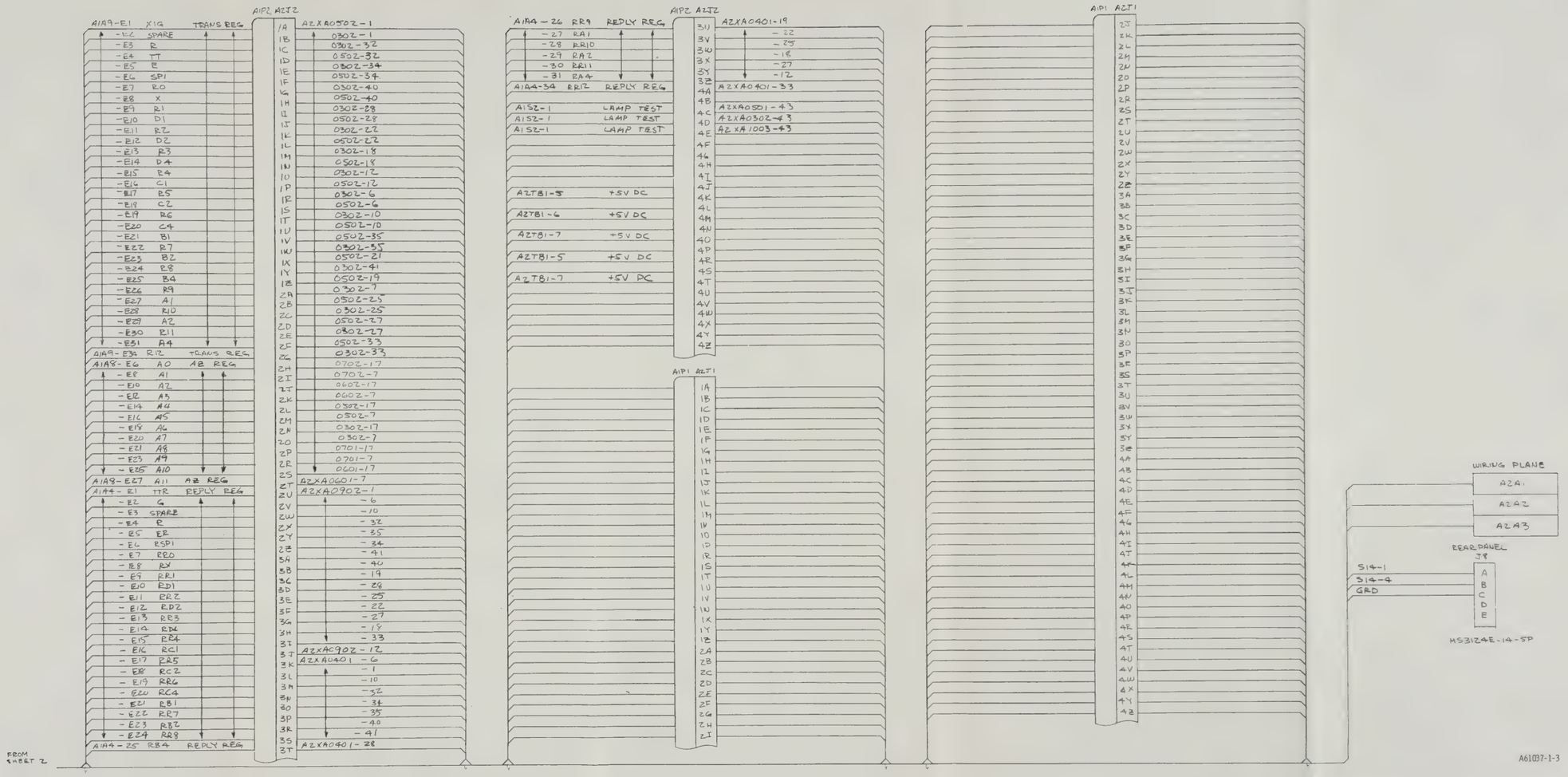
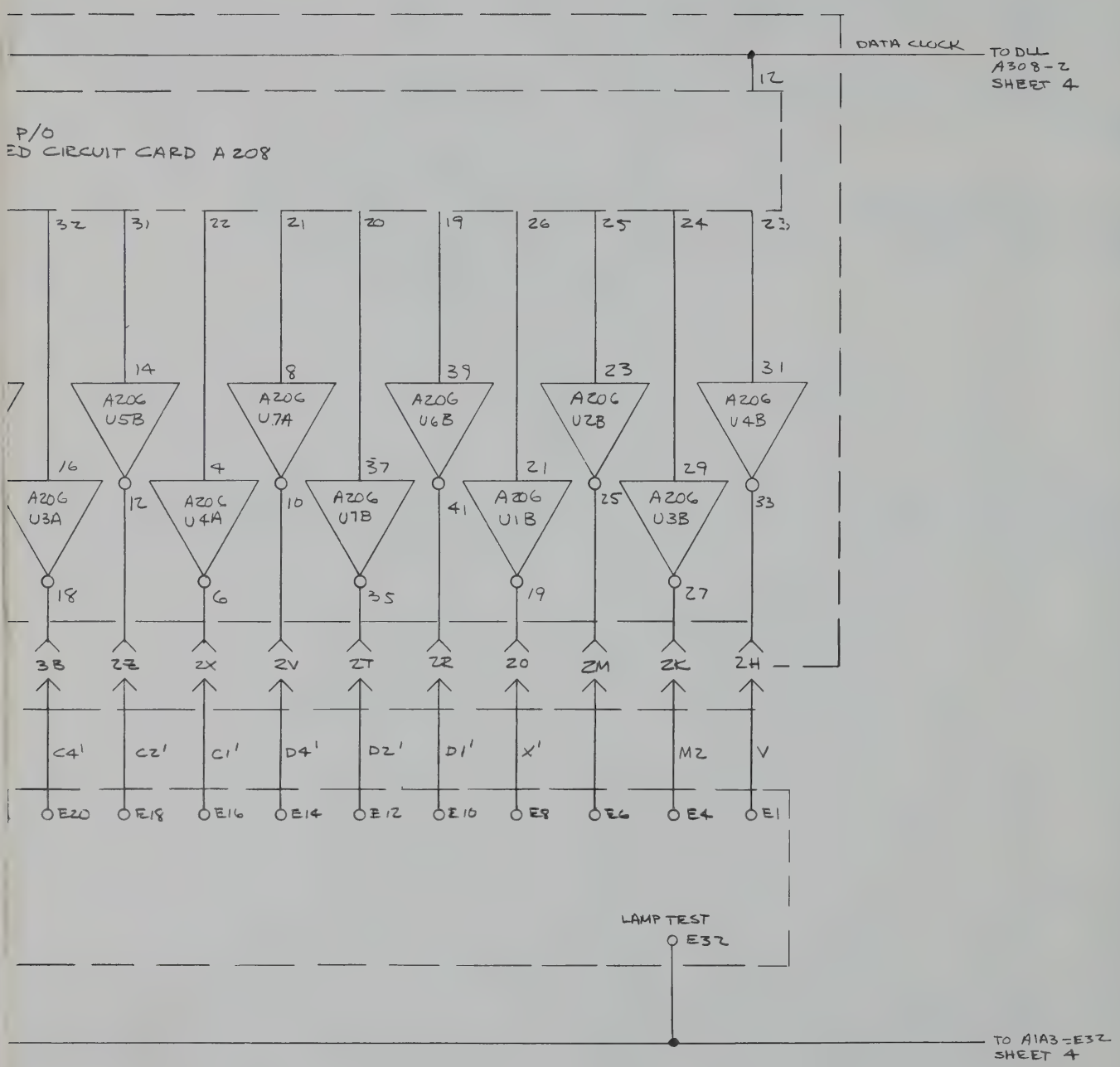
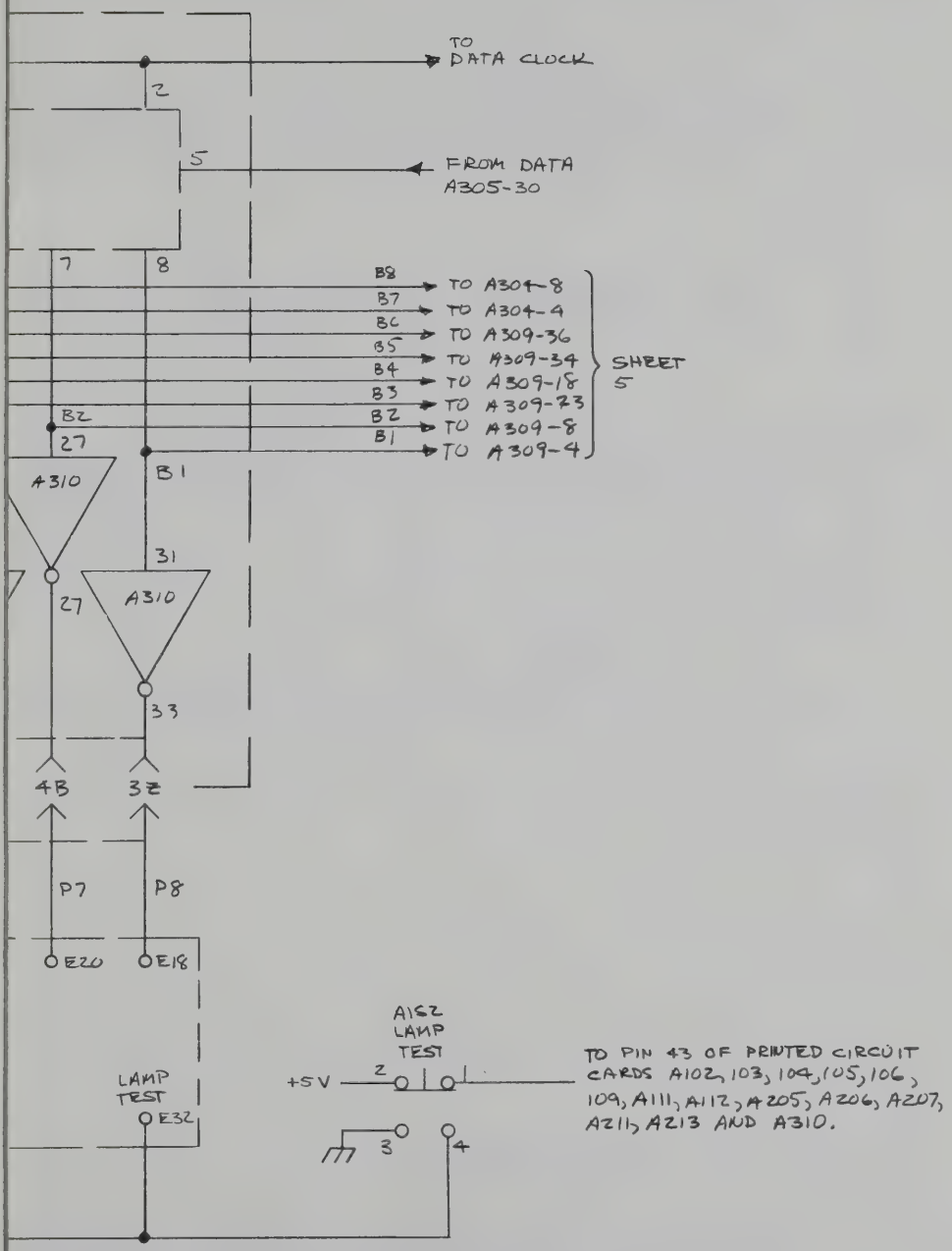


FIGURE 1. VIDEO SIGNAL PROCESSOR TEST SET SCHEMATIC WIRING DIAGRAM (SHEET 3 OF 3)

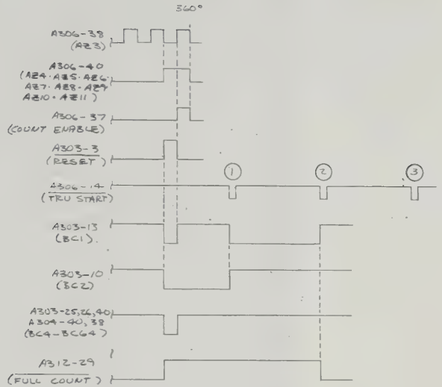

DATA CLOCK
TO DLL
A308-2
SHEET 4
12
P/O
ED CIRCUIT CARD A208
32 31 22 21 20 19 26 25 24 23
A206 U5B
A206 U7A
A206 U6B
A206 U2B
A206 U4B
A206 U3A
A206 U4A
A206 U7B
A206 U1B
A206 U3B
3B 2Z 2X 2V 2T 2R 2D 2M 2K 2H
C4' C2' C1' D4' D2' D1' X' M2 V
E20 E18 E16 E14 E12 E10 E8 E6 E4 E1
LAMP TEST
E32
TO A1A3-E32
SHEET 4

A61037-2-3



A61037-2-4

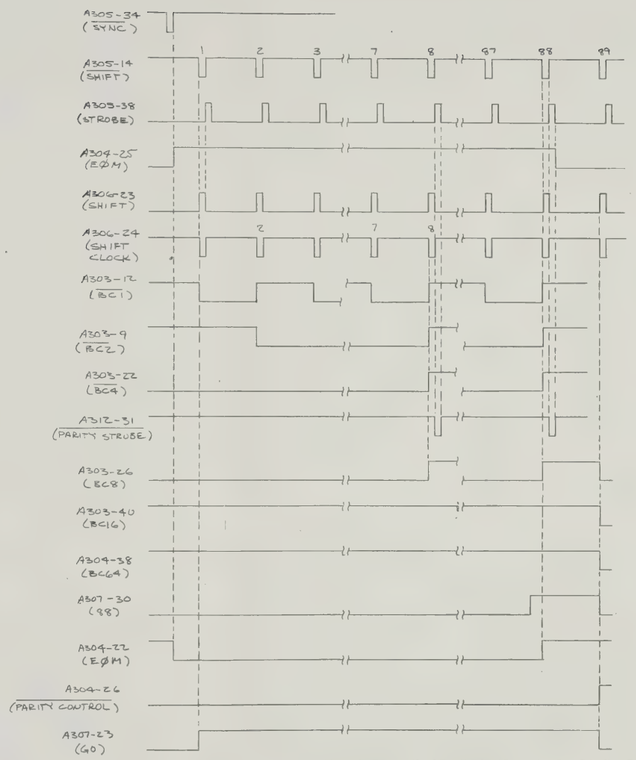
FIGURE 2. VIDEO SIGNAL PROCESSOR TEST SET OVERALL LOGIC DIAGRAM (SHEET 4 OF 11)



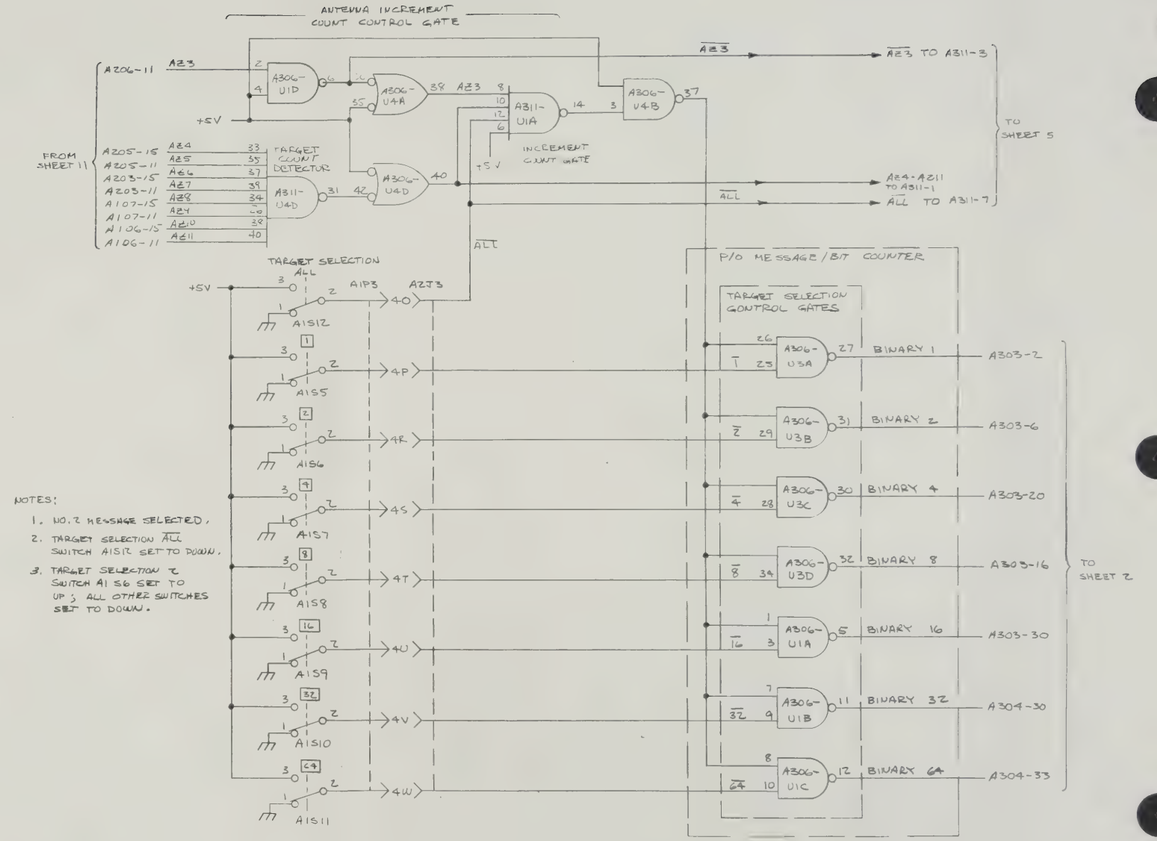
MESSAGE SELECTION TIMING SEQUENCE

NOTES:

1. NO. 2 MESSAGE SELECTED.
2. TARGET SELECTION $\overline{ALL}$ SWITCH A1S12 SET TO DOWN.
3. TARGET SELECTION 2 SWITCH A1S6 SET TO UP; ALL OTHER SWITCHES SET TO DOWN.



BIT COUNTING, PARITY STROBE, END OF MESSAGE TIMING SEQUENCE

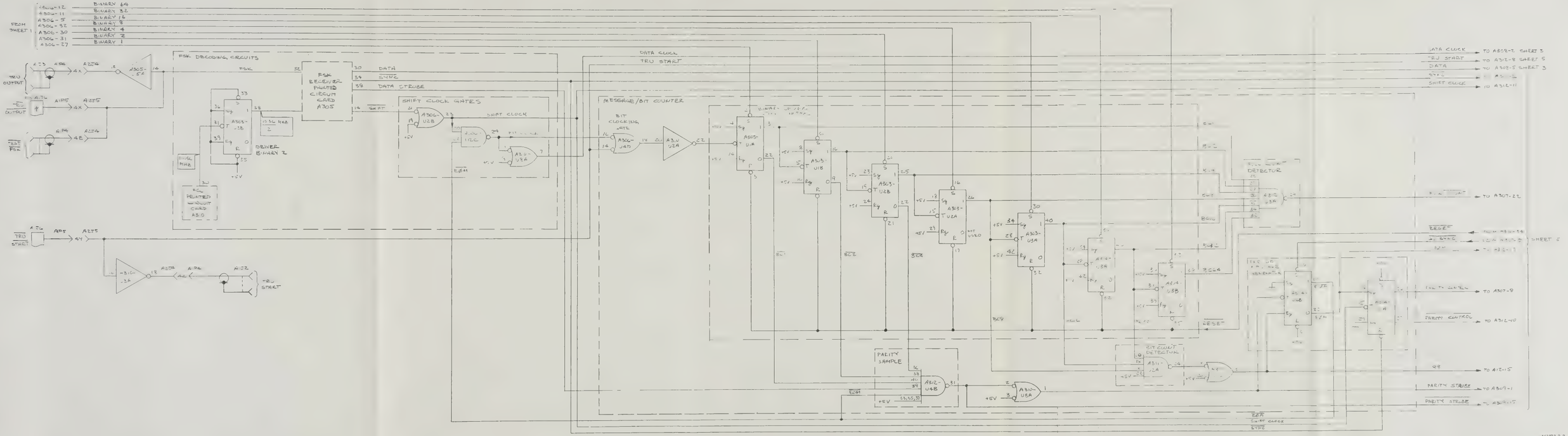


NOTES:

1. NO. 2 MESSAGE SELECTED.
2. TARGET SELECTION $\overline{ALL}$ SWITCH A1S12 SET TO DOWN.
3. TARGET SELECTION 2 SWITCH A1S6 SET TO UP; ALL OTHER SWITCHES SET TO DOWN.

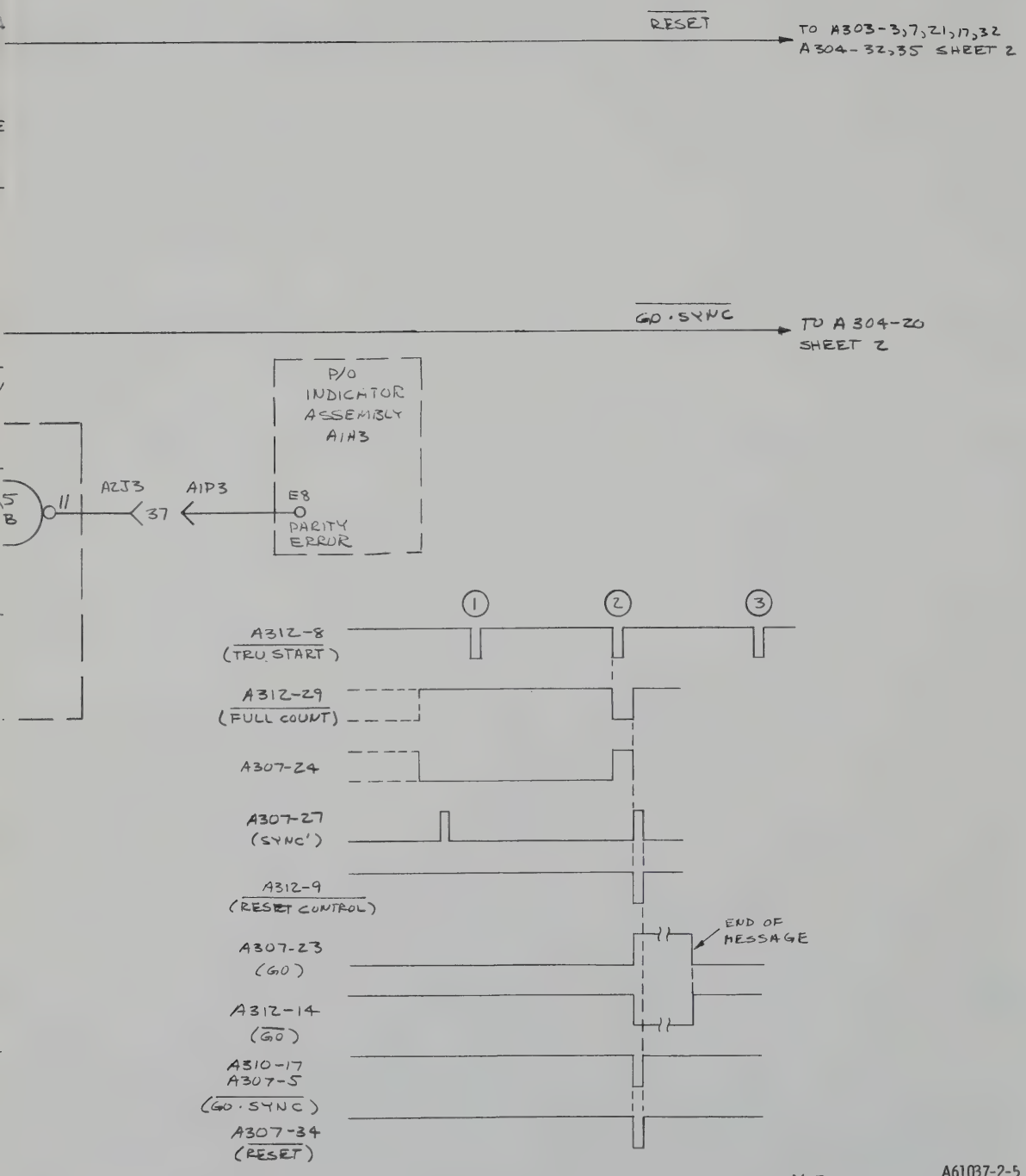
A61037-2-1

FIGURE 2. VIDEO SIGNAL PROCESSOR TEST SET OVERALL LOGIC DIAGRAM (SHEET 1 OF 11)



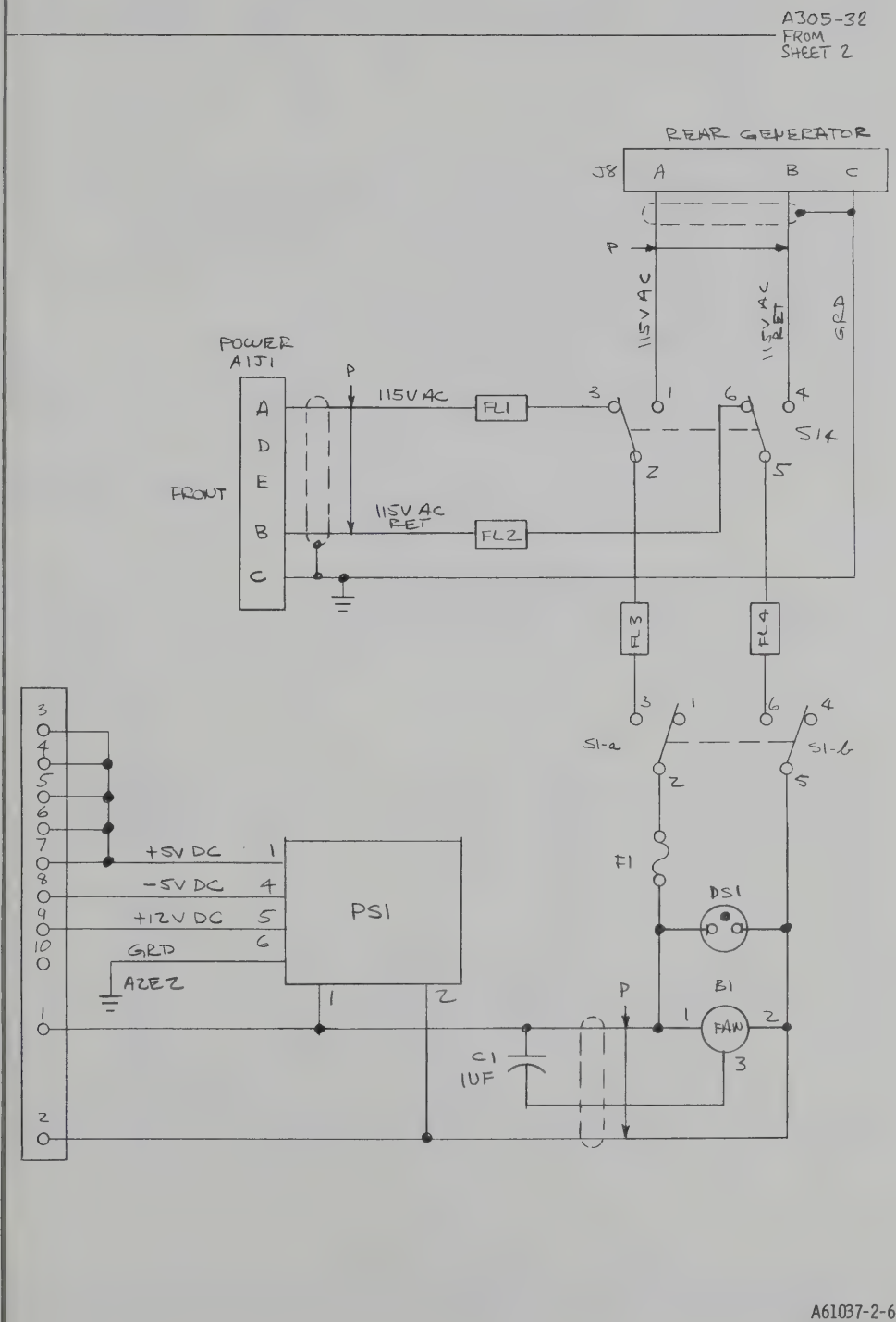
A61037-2-2

FIGURE 2. VIDEO SIGNAL PROCESSOR TEST SET OVERALL LOGIC DIAGRAM (SHEET 2 OF 11)



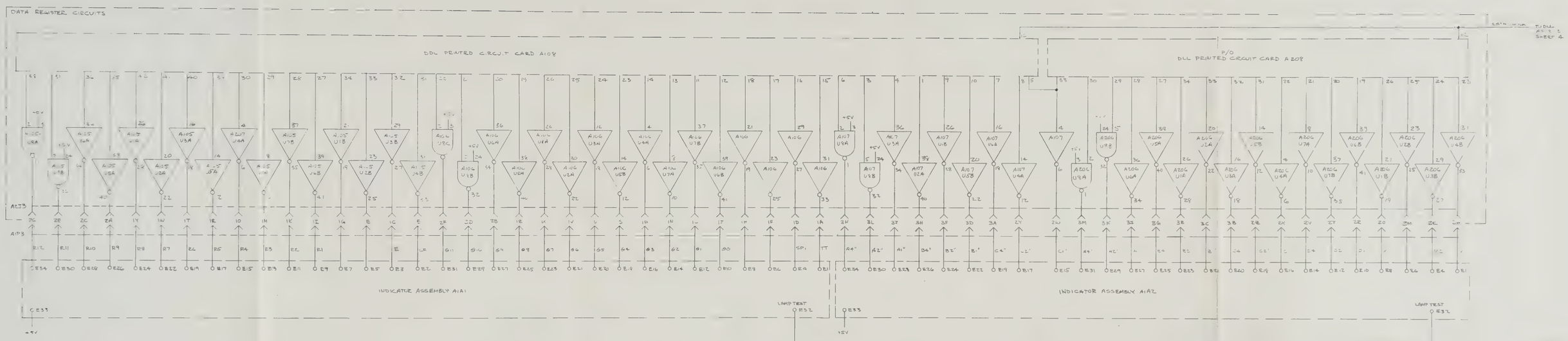
COUNTER RESET CONTROL TIMING SEQUENCE

A61037-2-5



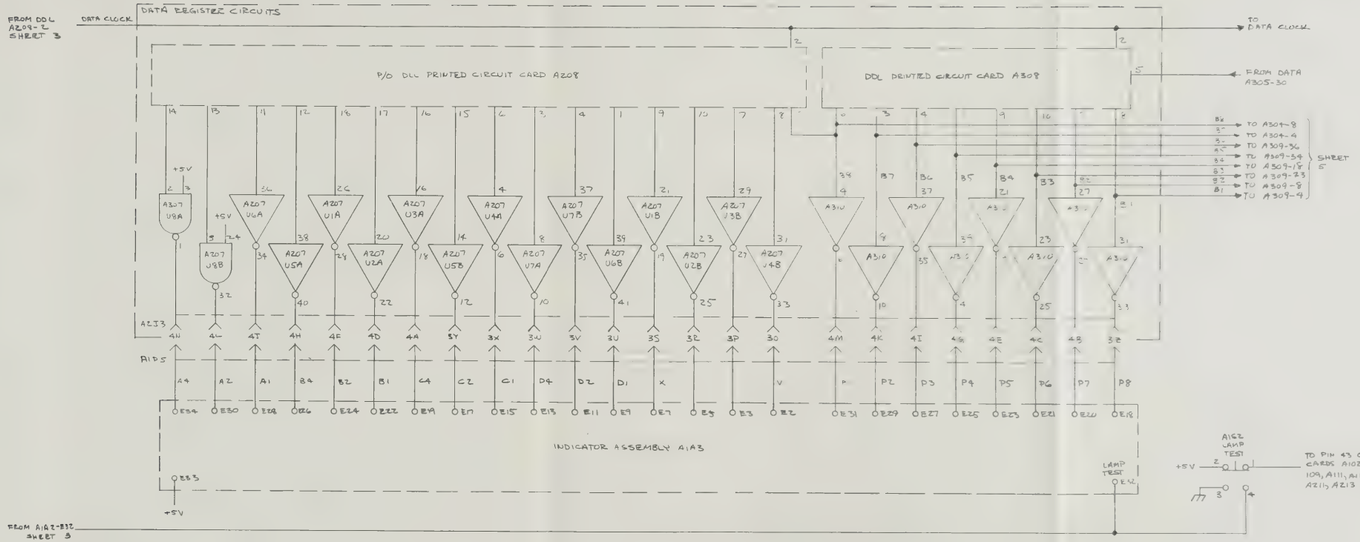
A61037-2-6

FIGURE 2. VIDEO SIGNAL PROCESSOR TEST SET OVERALL LOGIC DIAGRAM (SHEET 6 OF 11)



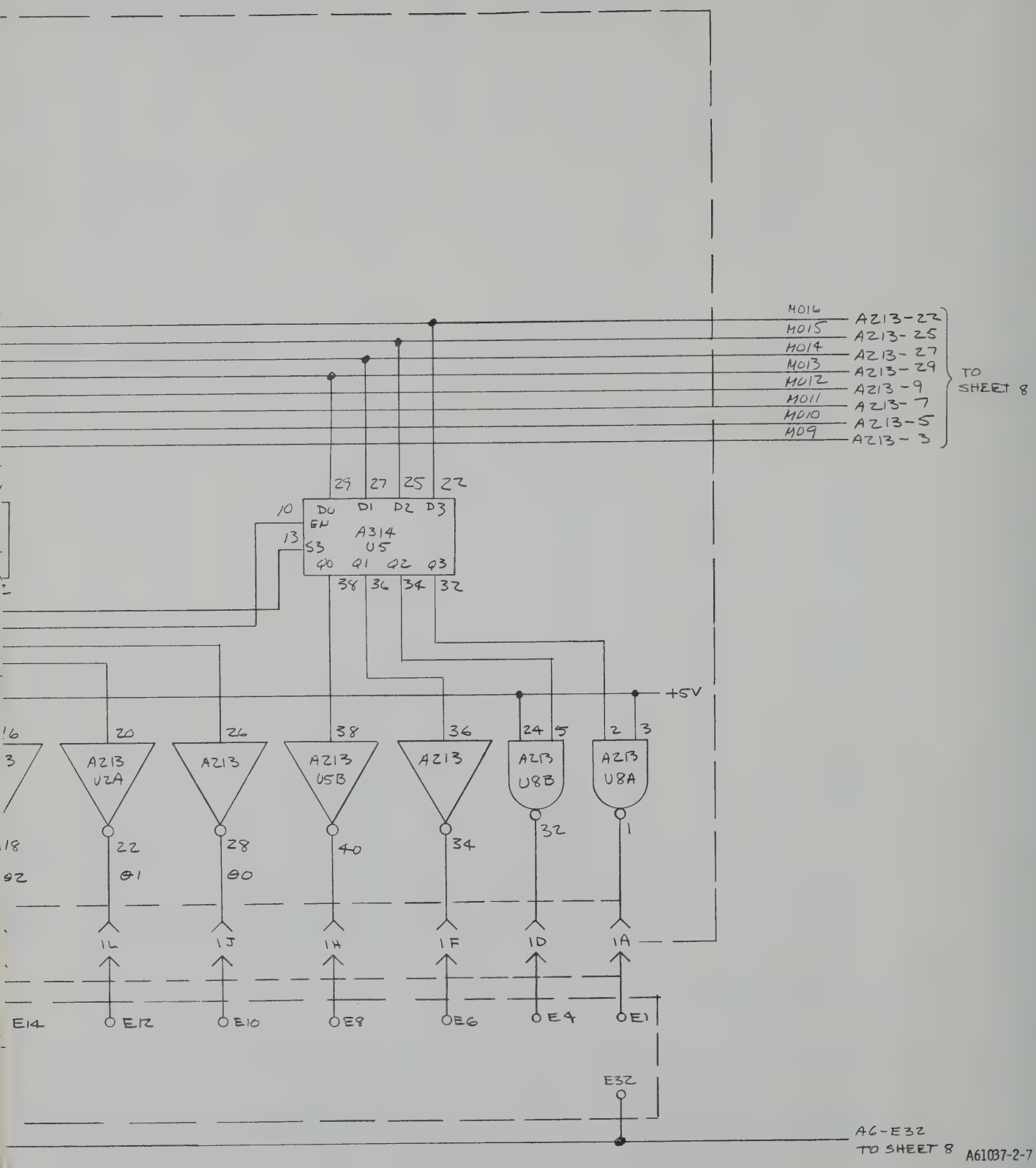
A61037-2-3

FIGURE 2. VIDEO SIGNAL PROCESSOR TEST SET OVERALL LOGIC DIAGRAM (SHEET 3 OF 11)

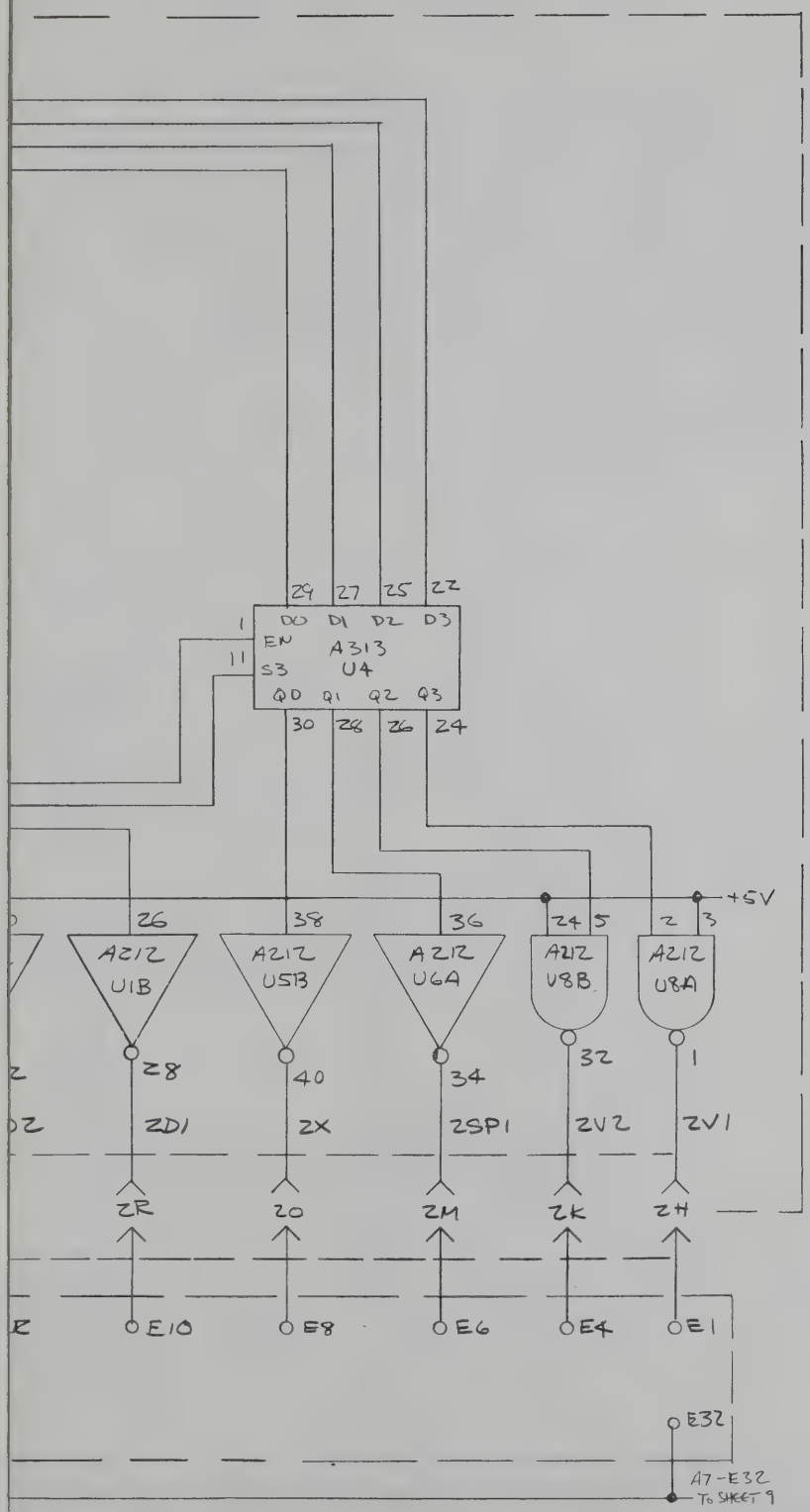


A61037-2-4

FIGURE 2. VIDEO SIGNAL PROCESSOR TEST SET OVERALL LOGIC DIAGRAM (SHEET 4 OF 11)


MD16
MD15
MD14
MD13
MD12
MD11
MD10
MD09
AZ13-22
AZ13-25
AZ13-27
AZ13-29
AZ13-9
AZ13-7
AZ13-5
AZ13-3
TO SHEET 8
29 27 25 22
10 DO D1 D2 D3
EN
13 S3 A314 U5
Q0 Q1 Q2 Q3
38 36 34 32
+5V
20 26 38 36 24 5 2 3
AZ13 U2A
AZ13
AZ13 U5B
AZ13
AZ13 U8B
AZ13 U8A
22 28 40 34 32 1
Q1 Q0
1L 1J 1H 1F 1D 1A
E14 E12 E10 E8 E6 E4 E1
E32
A6-E32
TO SHEET 8

A61037-2-7



A61037-2-8

FIGURE 2. VIDEO SIGNAL PROCESSOR TEST SET OVERALL LOGIC DIAGRAM (SHEET 8 OF 11)

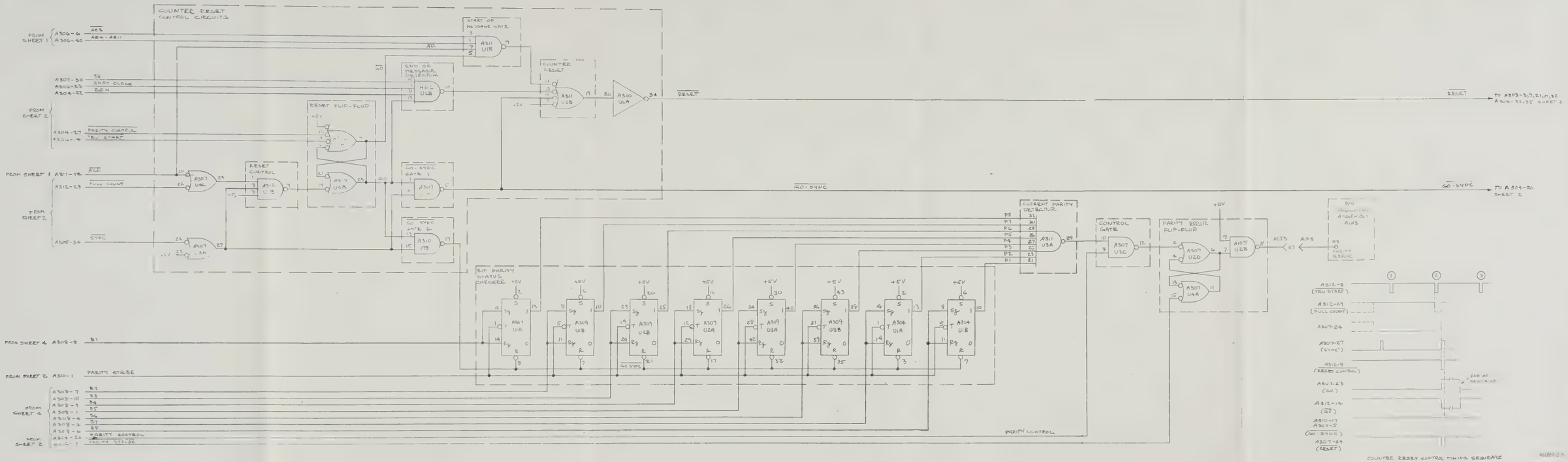
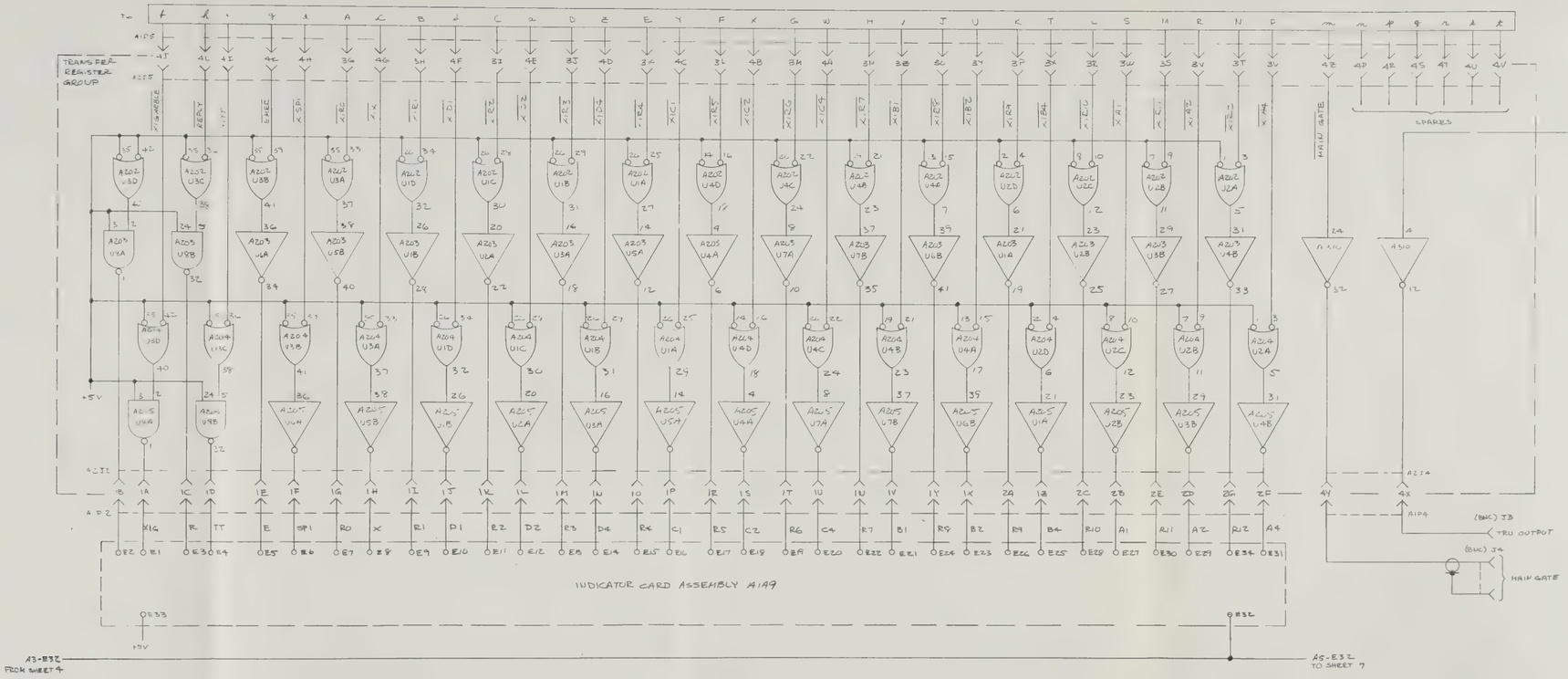
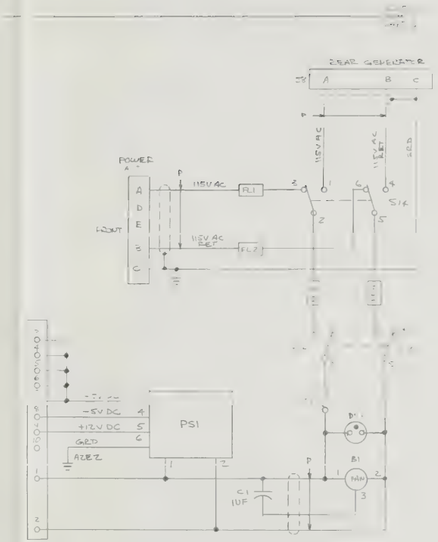


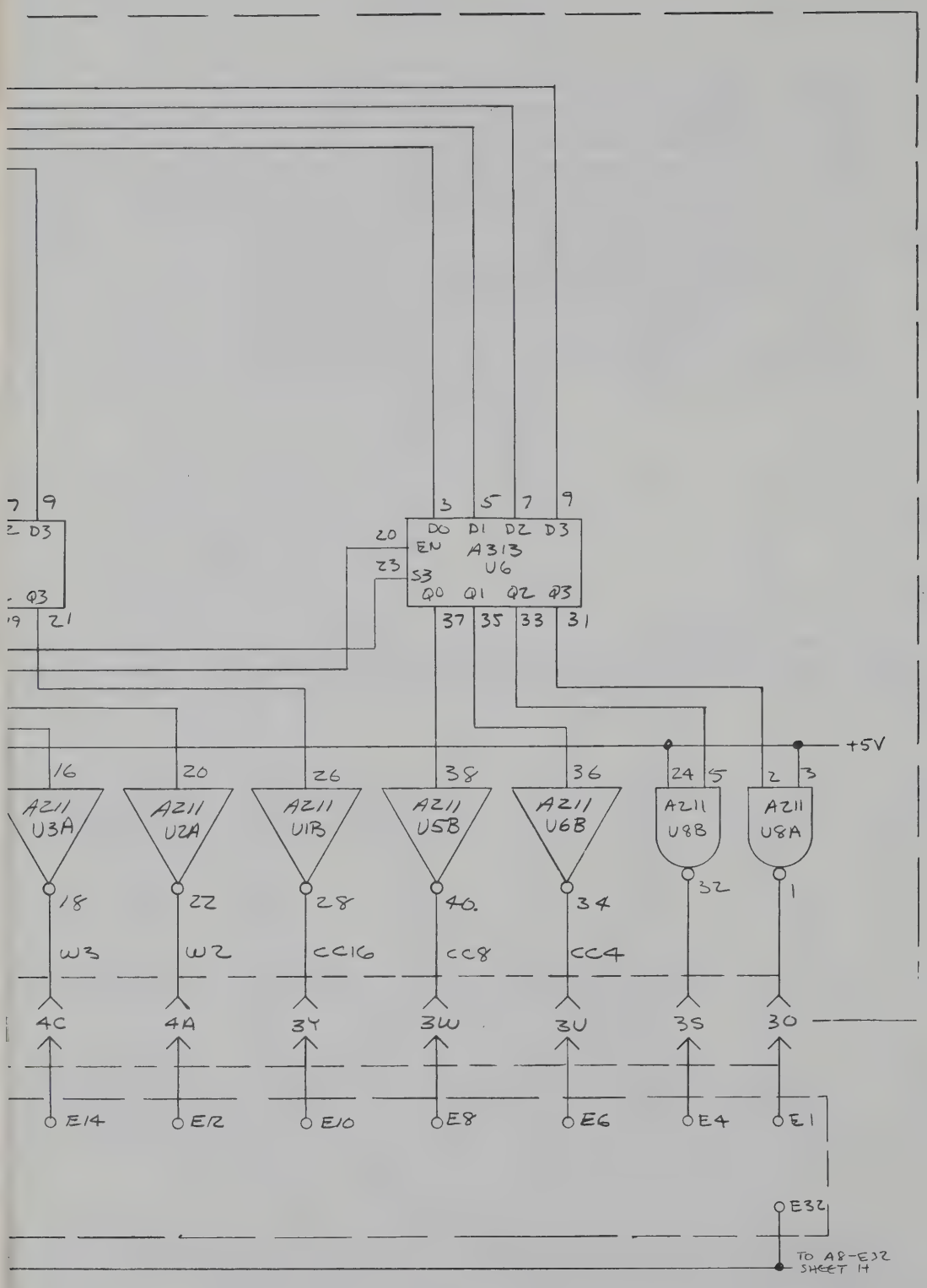
FIGURE 2. VIDEO SIGNAL PROCESSOR TEST SET OVERALL LOGIC DIAGRAM (SHEET 5 OF 11)





Ao1037-2-6

FIGURE 2. VIDEO SIGNAL PROCESSOR TEST SET OVERALL LOGIC DIAGRAM (SHEET 6 OF 11)


A313
U6
DO D1 D2 D3
EN
S3
Q0 Q1 Q2 Q3
+5V
A211 U3A
A211 U2A
A211 U1B
A211 U5B
A211 U6B
A211 U8B
A211 U8A
W3
W2
CC16
CC8
CC4
4C
4A
3Y
3W
3U
3S
3O
E14
E12
E10
E8
E6
E4
E1
E32
TO A8-E32 SHEET 14

A61037-2-9

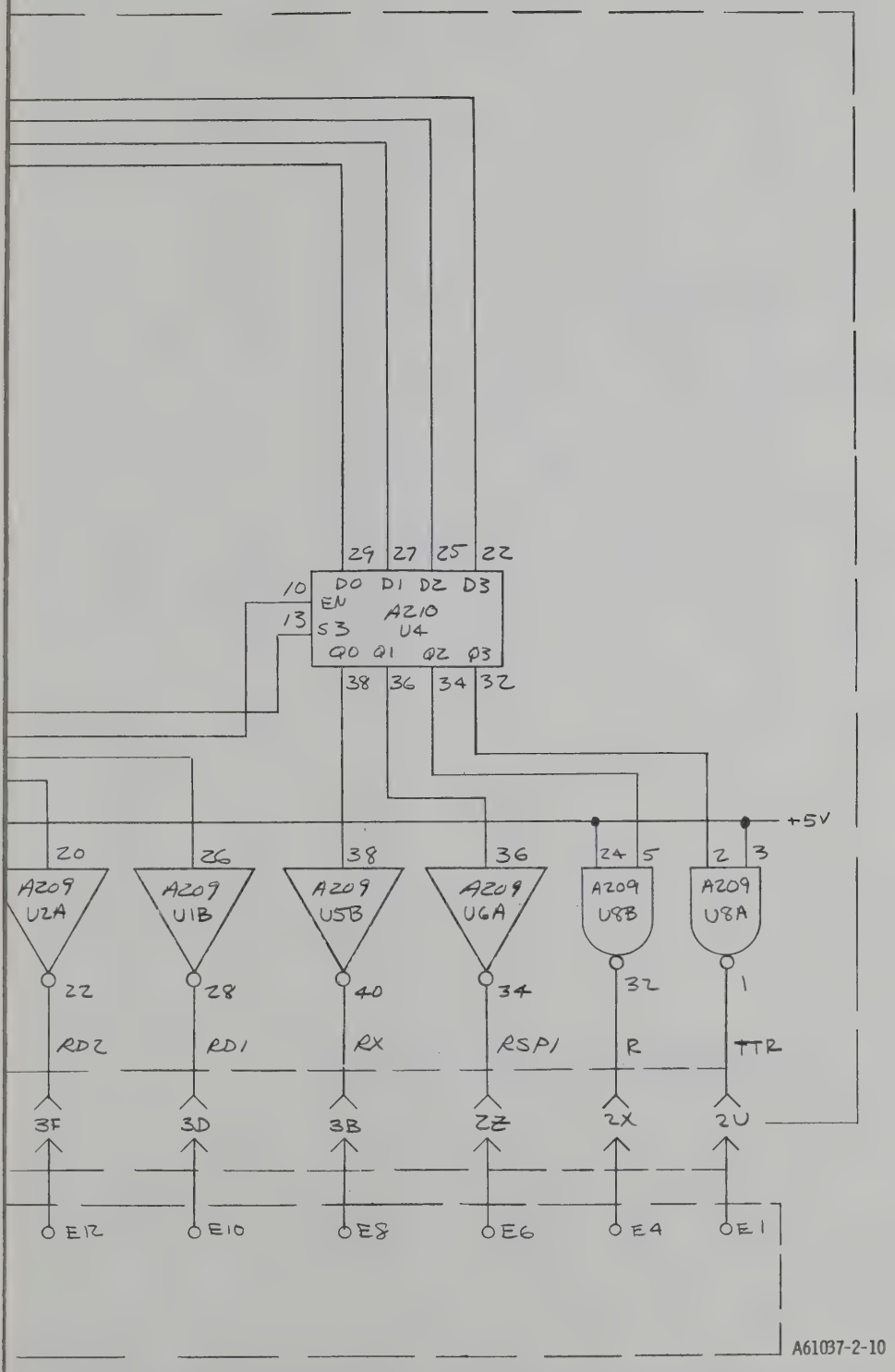


FIGURE 2. VIDEO SIGNAL PROCESSOR TEST SET OVERALL LOGIC DIAGRAM (SHEET 10 OF 11)

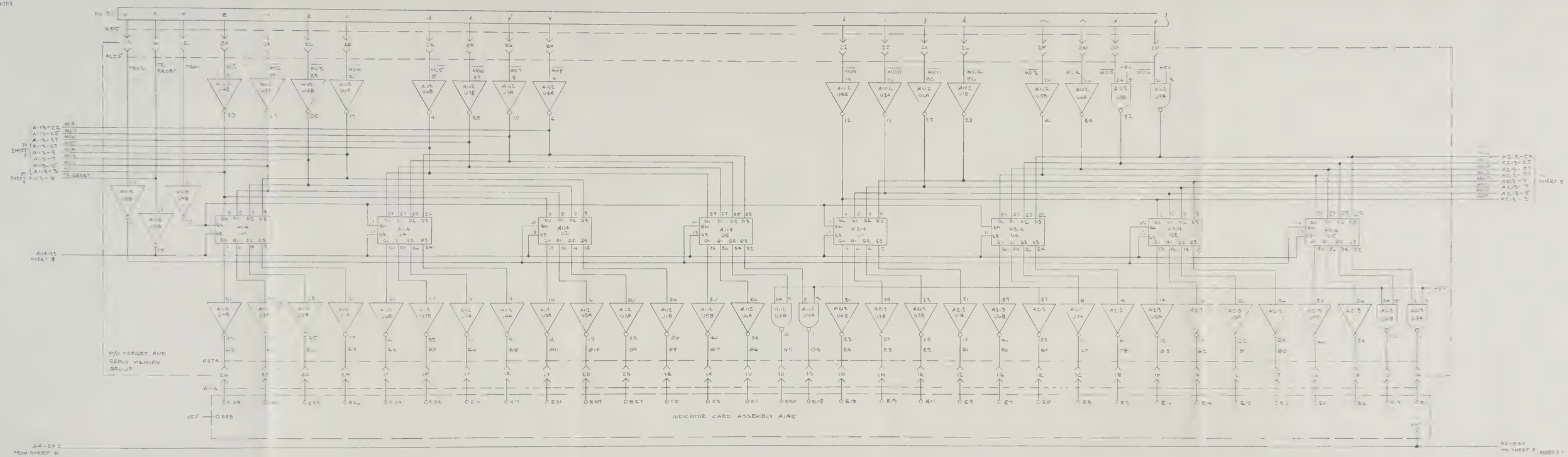
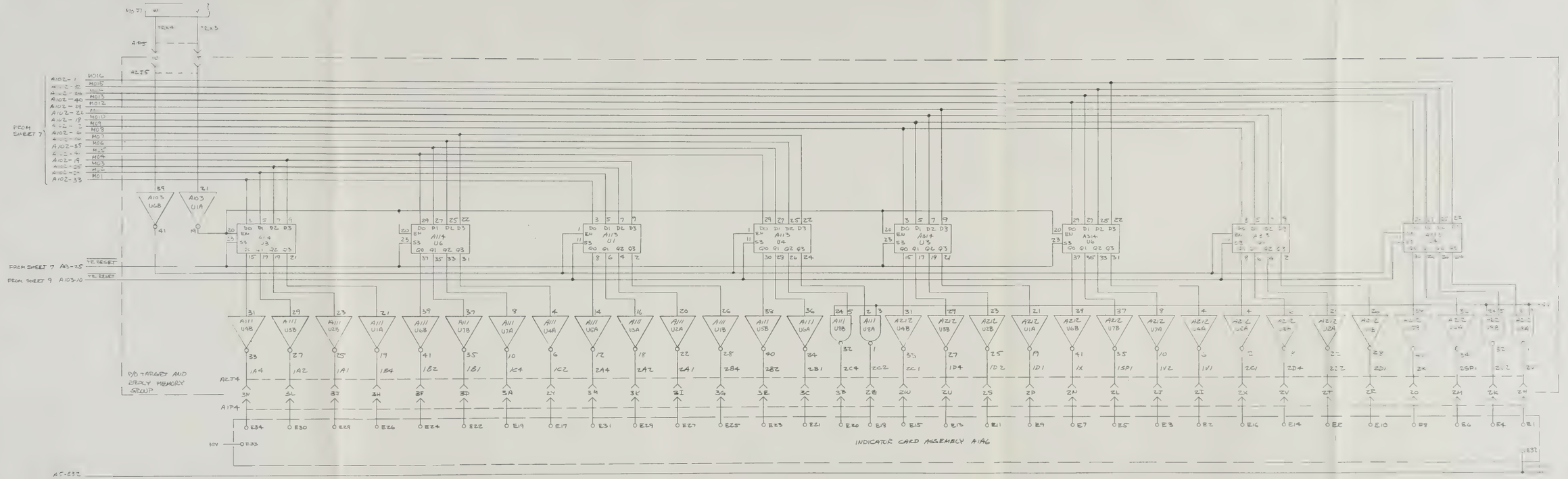
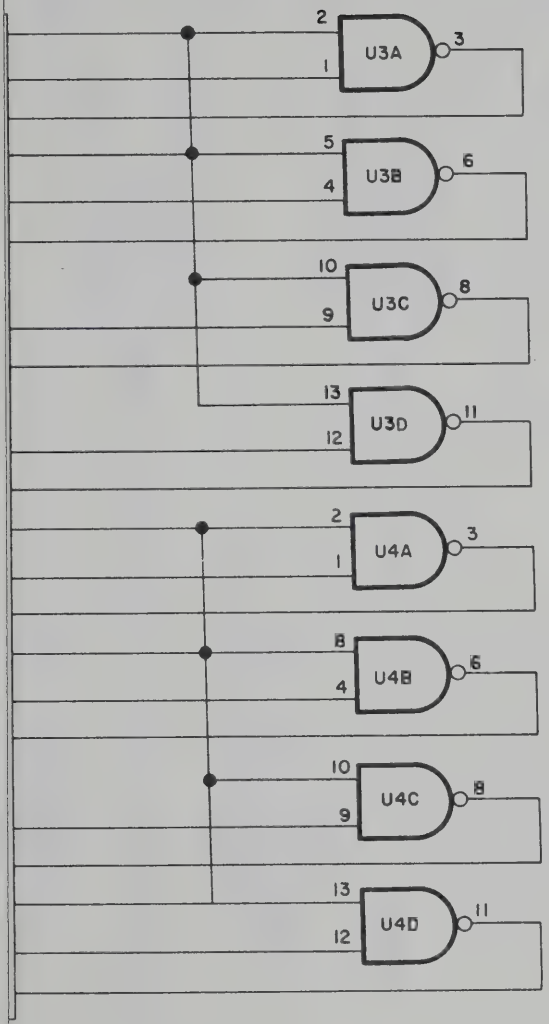


FIGURE 2. VIDEO SIGNAL PROCESSOR TEST SET OVERALL LOGIC DIAGRAM (SHEET 7 OF 11)


FROM SHEET 7
FROM SHEET 7 A03-25
FROM SHEET 9 A103-10
B/D TARGET AND EARLY MEMORY GROUP
INDICATOR CARD ASSEMBLY A1A6
A6-E37 FROM SHEET 7

A6L037-2-8

FIGURE 2. VIDEO SIGNAL PROCESSOR TEST SET OVERALL LOGIC DIAGRAM (SHEET 8 OF 11)



ND U4 ARE QUADRUPLE
SITIVE NAND GATES.
FERENCE DESIGNATIONS ARE SHOWN
ETE PREFIX WITH NUMBER OR SUBASSEMBLY
N.

A61037-3

FIGURE 3. GTT, CIRCUIT CARD SCHEMATIC

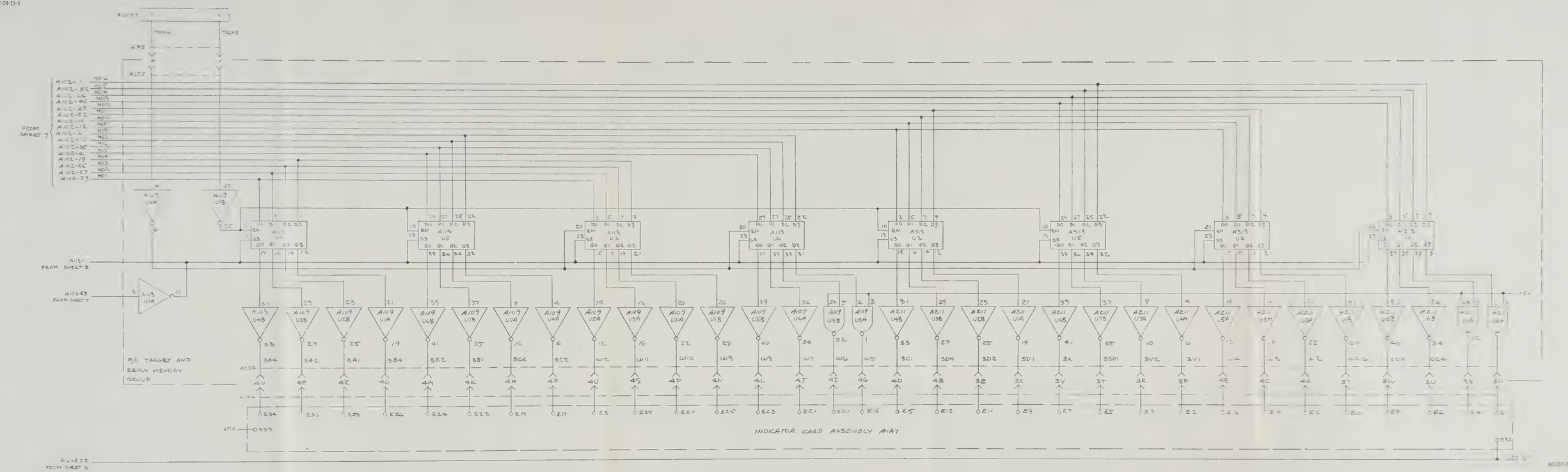
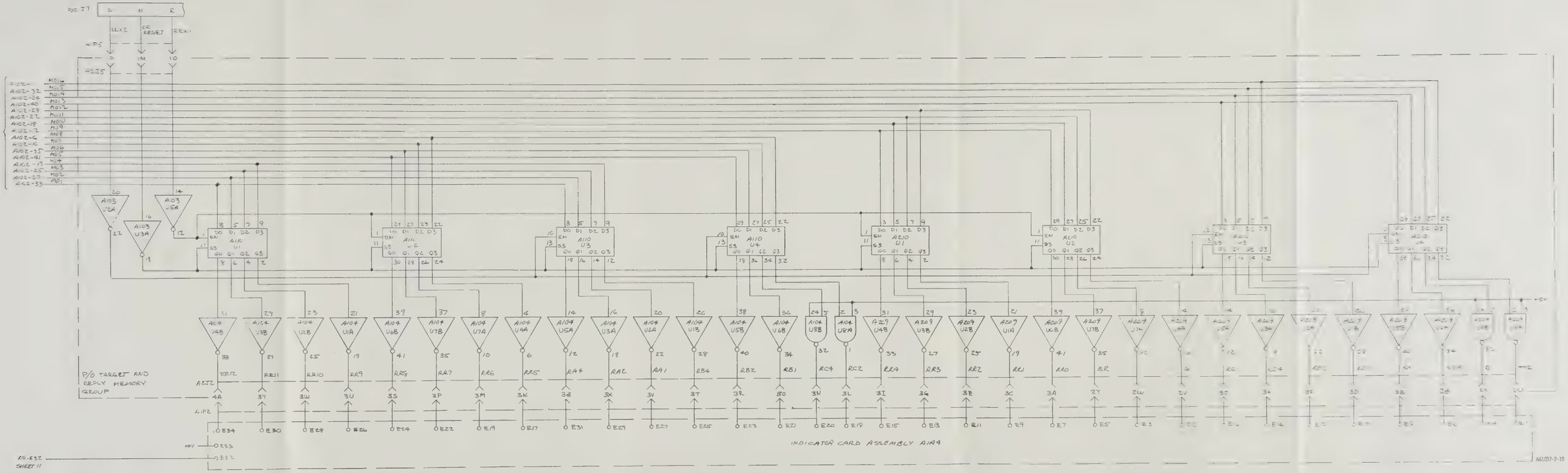
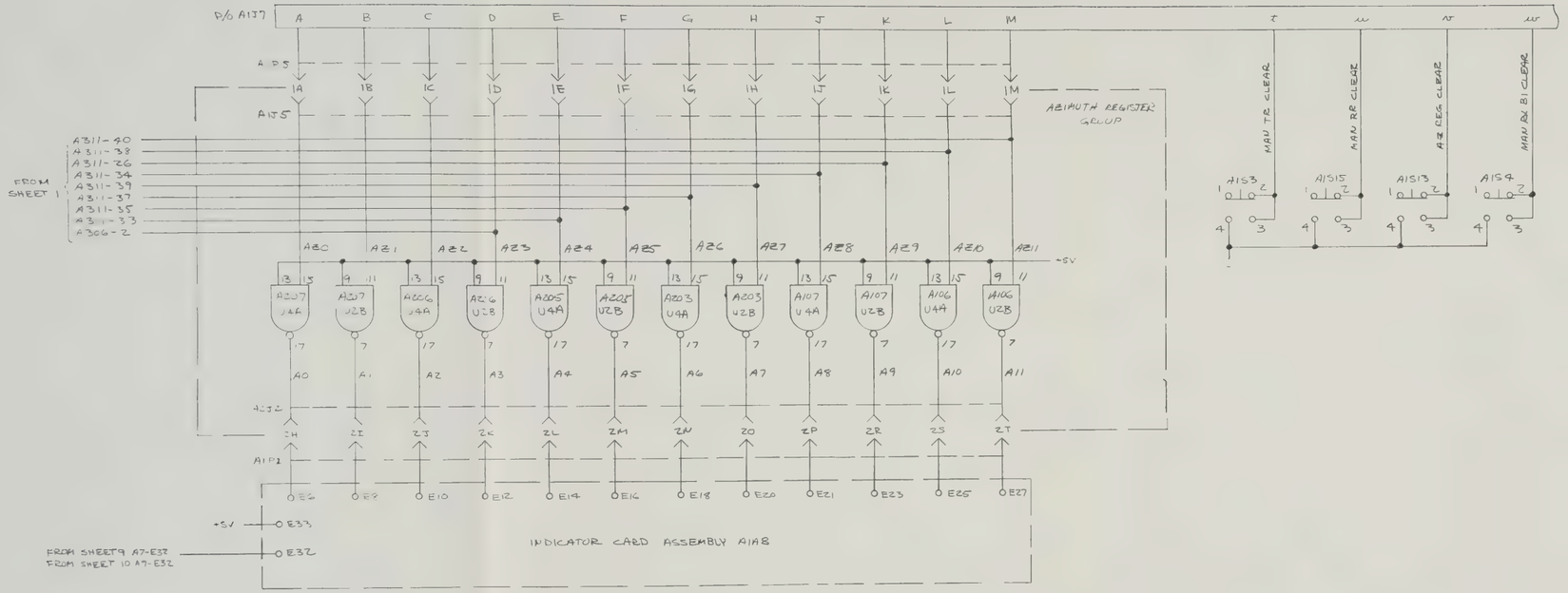


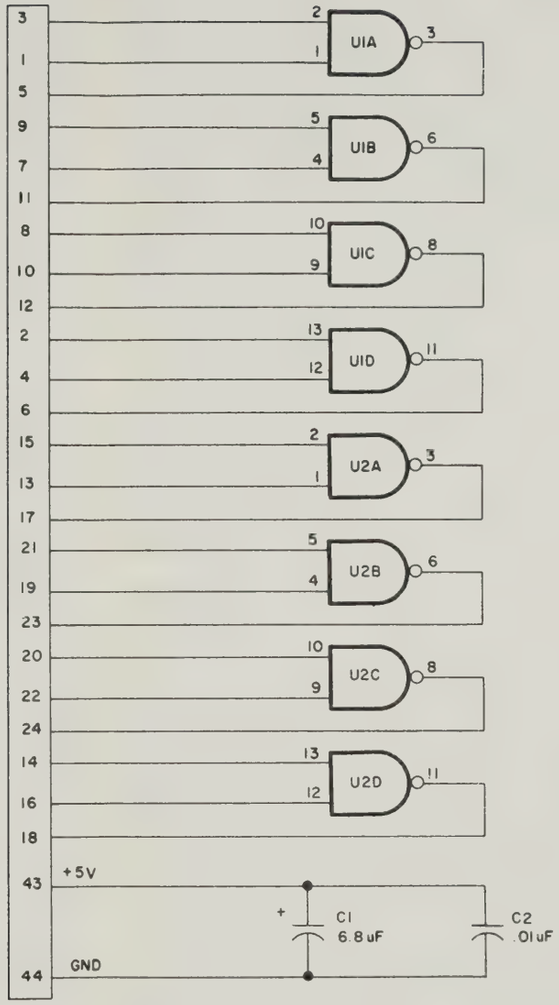
FIGURE 2. VIDEO SIGNAL PROCESSOR TEST SET OVERALL LOGIC DIAGRAM (SHEET 9 OF 11)


P/O J7
S
N
R
LEAD
RESET
REAR
+5V
10
1M
10
A102-32
A102-24
A102-40
A102-28
A102-22
A102-18
A102-7
A102-6
A102-15
A102-35
A102-41
A102-19
A102-25
A102-37
A102-33
FROM SHEET 7
A103 U2A
A103 U3A
A103 U5A
A11 U1
A11 U2
A10 U3
A10 U4
A29 U1
A29 U2
A104 U4B
A104 U3B
A104 U2B
A104 U1A
A104 U6B
A104 U7B
A104 U7A
A104 U6A
A104 U5A
A104 U3A
A104 U2A
A104 U1B
A104 U5B
A104 U6B
A104 U8B
A104 U8A
A29 U4B
A29 U3B
A29 U2B
A29 U1A
A29 U6B
A29 U7B
A29 U7A
A29 U6A
A29 U5A
A29 U3A
A29 U2A
A29 U1B
A29 U5B
A29 U4B
A29 U3B
A29 U2B
A29 U1A
A29 U6B
A29 U7B
A29 U7A
A29 U6A
A29 U5A
A29 U3A
A29 U2A
A29 U1B
A29 U5B
A29 U4B
A29 U3B
A29 U2B
A29 U1A
A29 U6B
A29 U7B
A29 U7A
A29 U6A
A29 U5A
A29 U3A
A29 U2A
A29 U1B
A29 U5B
A29 U4B
A29 U3B
A29 U2B
A29 U1A
+5V
P/O TARGET AND REPLY MEMORY GROUP
A1J2
4R
3Y
3W
3U
3S
3P
3M
3K
3E
3X
3V
3T
3R
3D
3N
3L
3I
3G
3E
3C
3A
2Y
2W
2V
3J
3H
3F
3D
3B
2Z
2X
2U
RR12
RR11
RR10
RR9
RR8
RR7
RR6
RR5
RA4
RA3
RA2
RA1
RB4
RB2
RB1
RC4
RC2

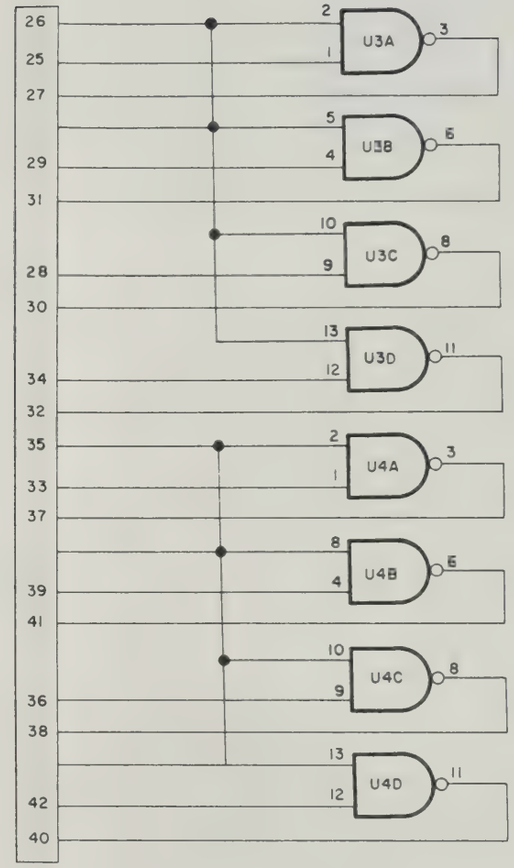


A61037-2-11

FIGURE 2. VIDEO SIGNAL PROCESSOR TEST SET OVERALL LOGIC DIAGRAM (SHEET 11 OF 11)



AIL PART NO. 373361-1

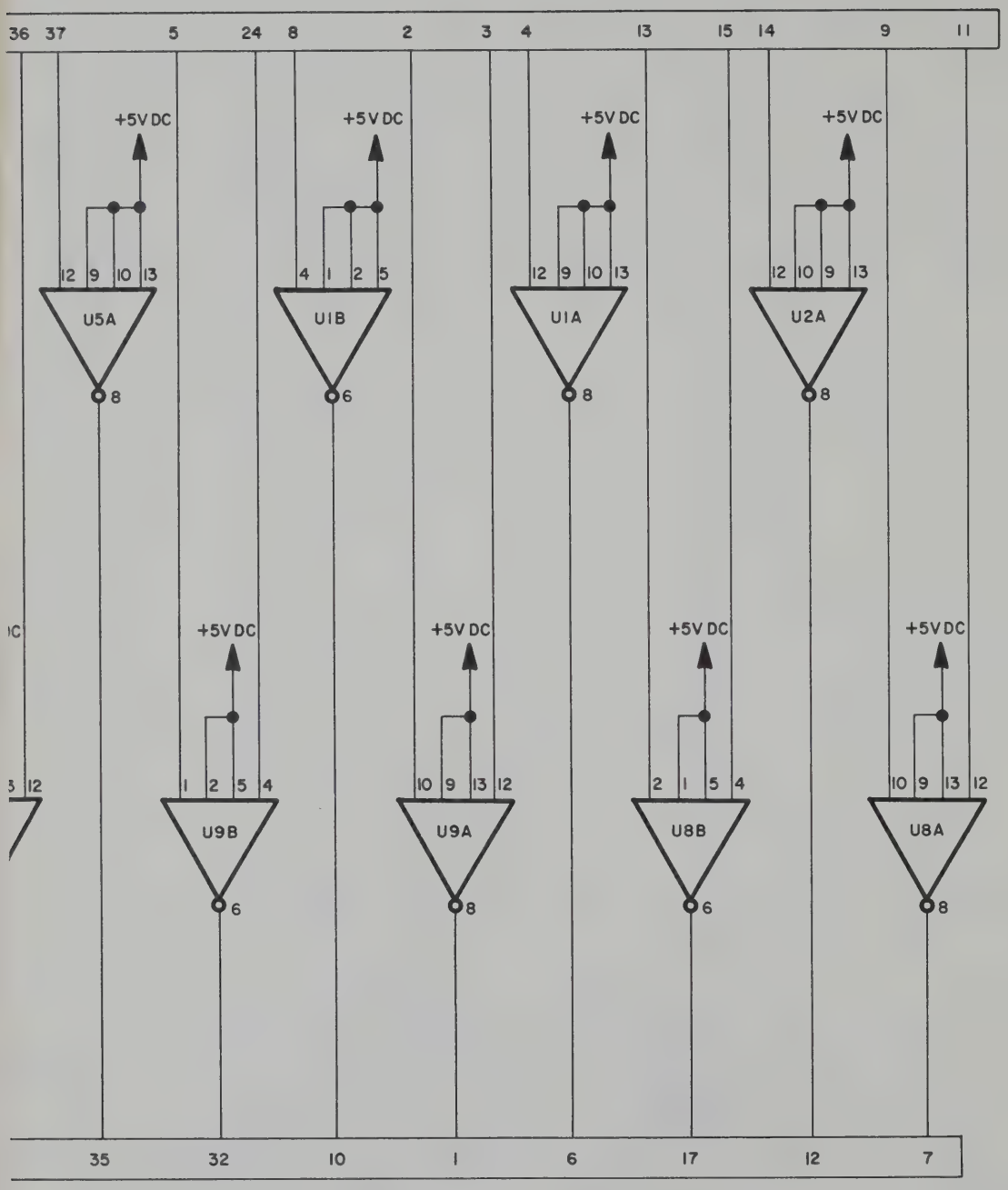


NOTES

1. U1,U2,U3 AND U4 ARE QUADRUPLE 2 INPUT POSITIVE NAND GATES
2. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN FOR COMPLETE PREFIX WITH NUMBER OR SUBASSEMBLY DESIGNATION

A61037-3

FIGURE 3. GTT, CIRCUIT CARD SCHEMATIC

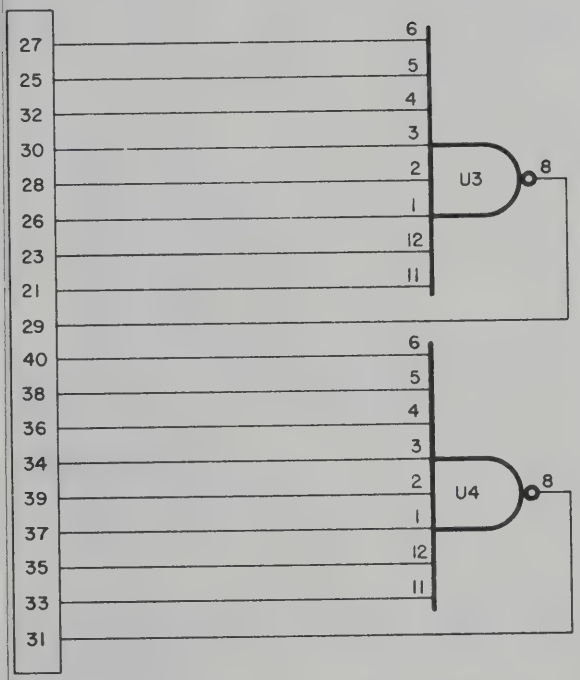


NOTES:

1. PIN 7 OF U1 THRU U9 IS CONNECTED TO GROUND. PIN 14 OF U1 THRU U9 IS CONNECTED TO +5V DC.
2. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN, FOR COMPLETE DESIGNATION PREFIX WITH UNIT NUMBER OR SUBASSEMBLY DESIGNATION.

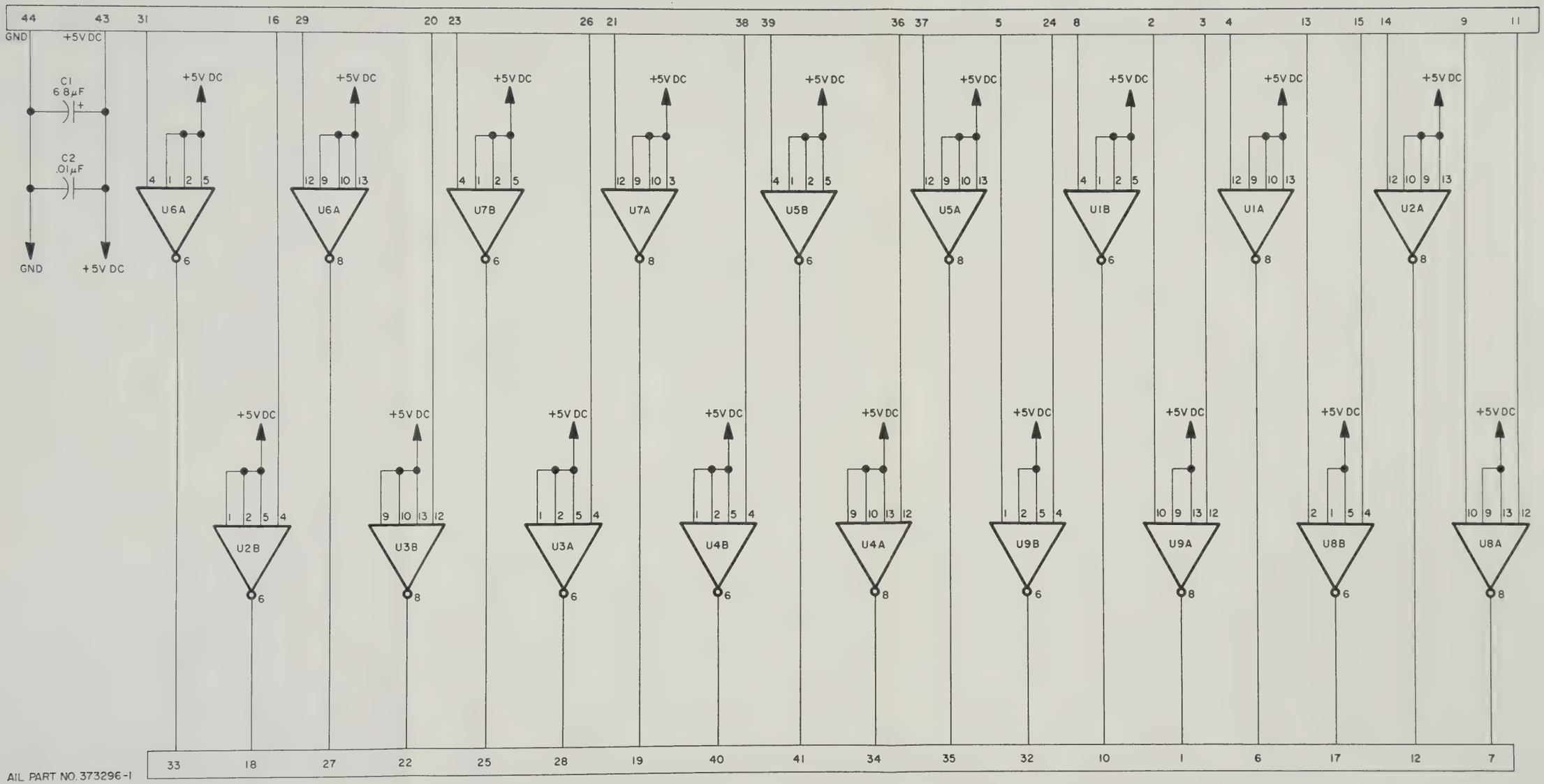
A61037-4

FIGURE 4. GTD, CIRCUIT CARD SCHEMATIC



A61037-5

FIGURE 5. GCT. CIRCUIT CARD SCHEMATIC



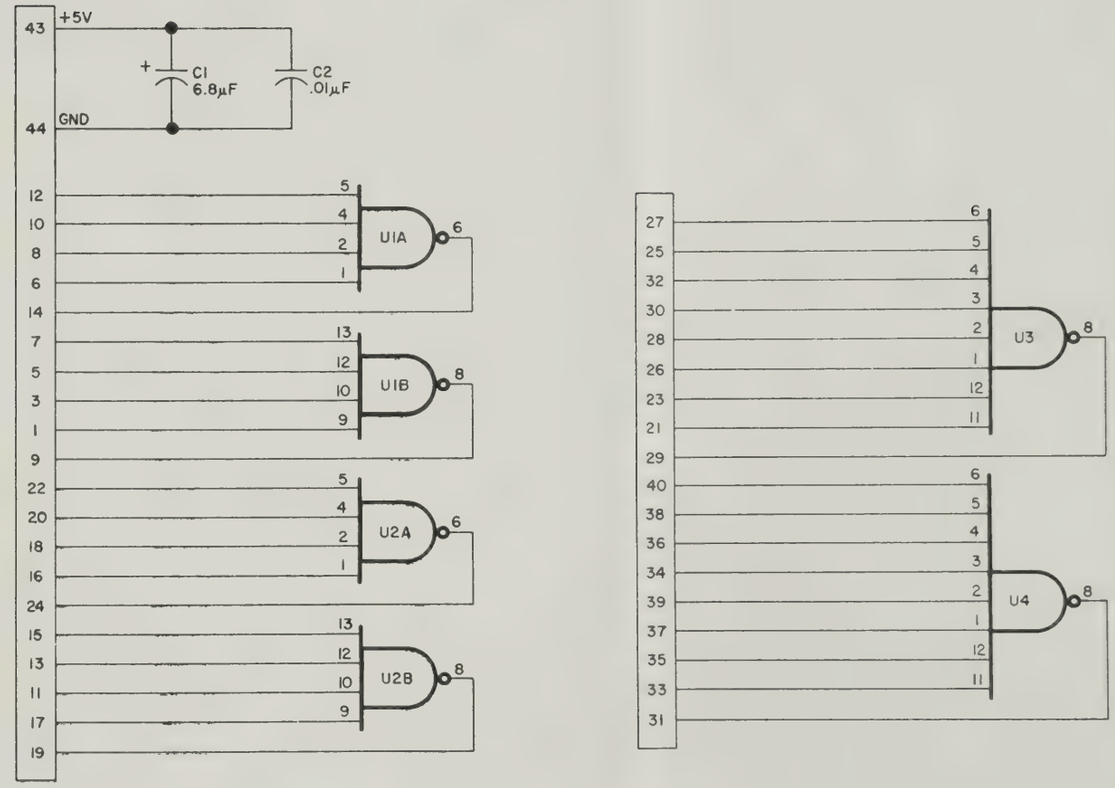
AIL PART NO. 373296-1

NOTES:

1. PIN 7 OF U1 THRU U9 IS CONNECTED TO GROUND. PIN 14 OF U1 THRU U9 IS CONNECTED TO +5V DC.
2. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN, FOR COMPLETE DESIGNATION PREFIX WITH UNIT NUMBER OR SUBASSEMBLY DESIGNATION.

A61037-4

FIGURE 4. GTD, CIRCUIT CARD SCHEMATIC



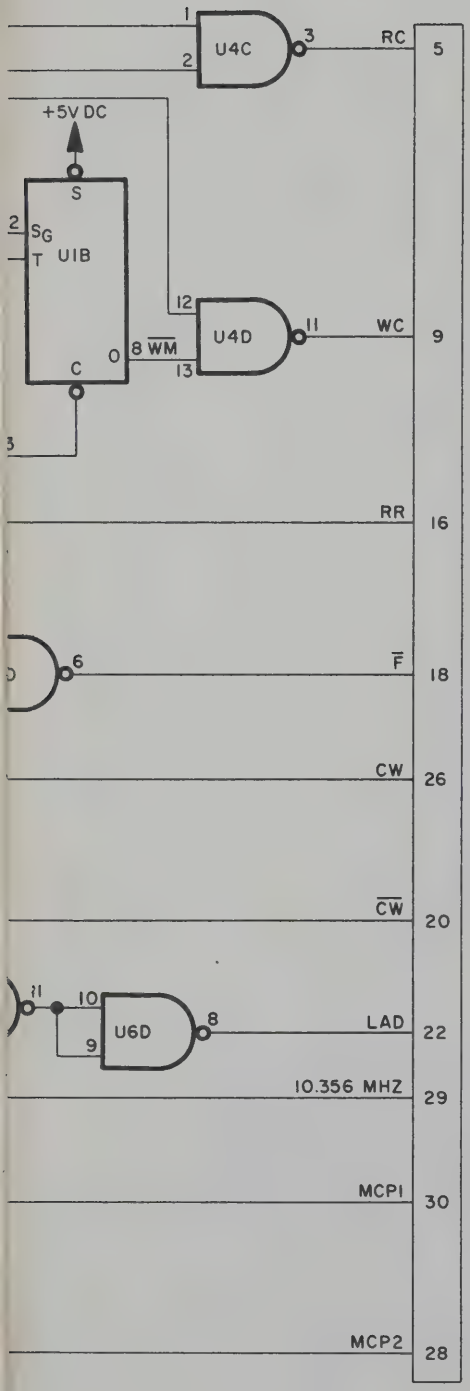
NOTES:

1. U1, U2 ARE DUAL 4 INPUT POSITIVE NAND GATES.
2. U3, U4 ARE 8 INPUT POSITIVE NAND GATES.
3. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN, FOR COMPLETE DESIGNATION PREFIX WITH UNIT NUMBER OR SUBASSEMBLY DESIGNATION.

AIL PART NO. 373359-1

A61037-5

FIGURE 5. GCT. CIRCUIT CARD SCHEMATIC



NOTES:

1. PIN 7 OF U1 IS CONNECTED TO GROUND.
   PIN 14 OF U1 THRU U7 IS CONNECTED TO +5V DC
2. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN FOR COMPLETE DESIGNATION PREFIX WITH UNIT NUMBER OR SUB ASSEMBLY DESIGNATION.

A61037-6

FIGURE 6. FCL, CIRCUIT CARD SCHEMATIC

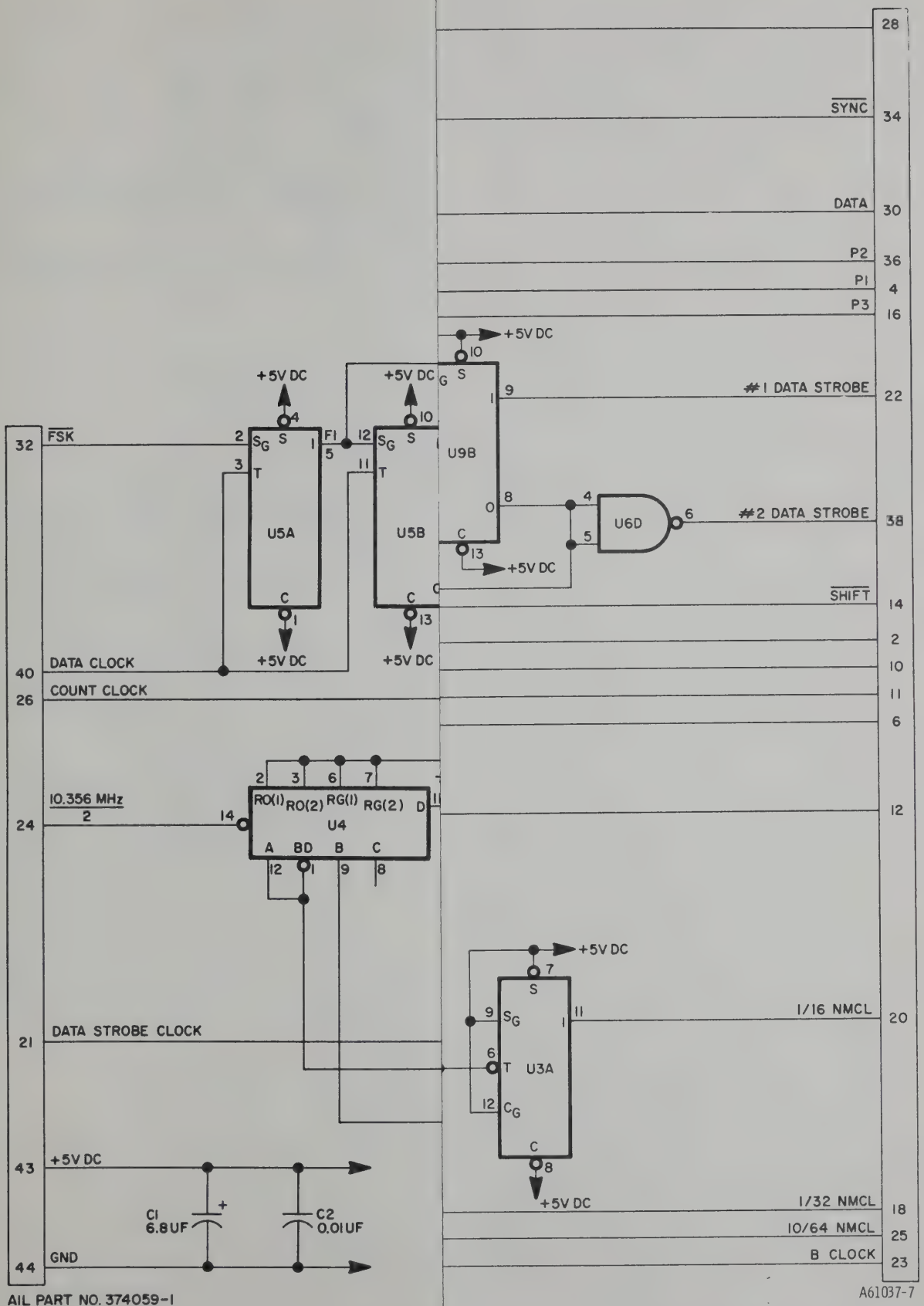
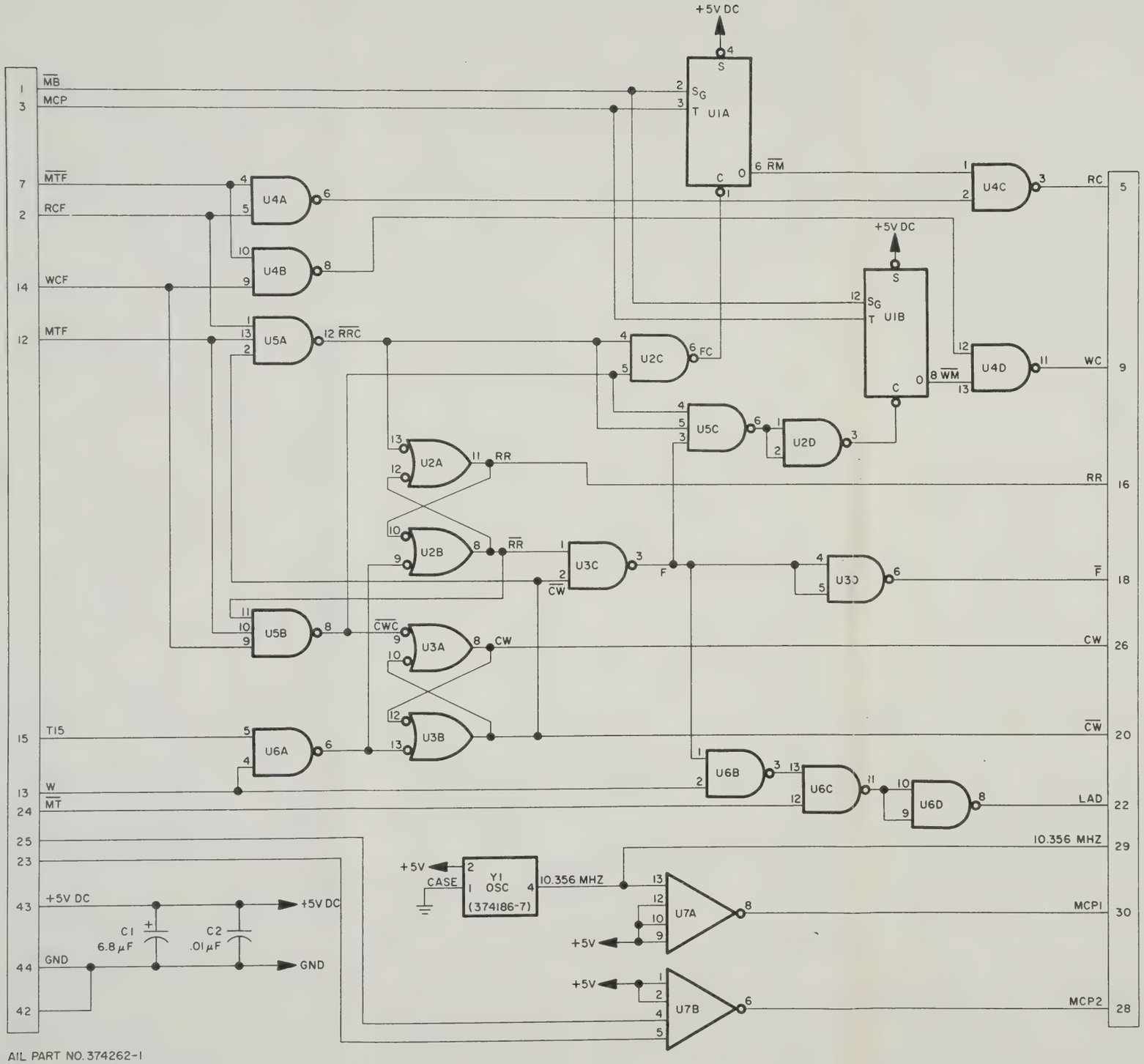


FIGURE 7. FSK, CIRCUIT CARD SCHEMATIC

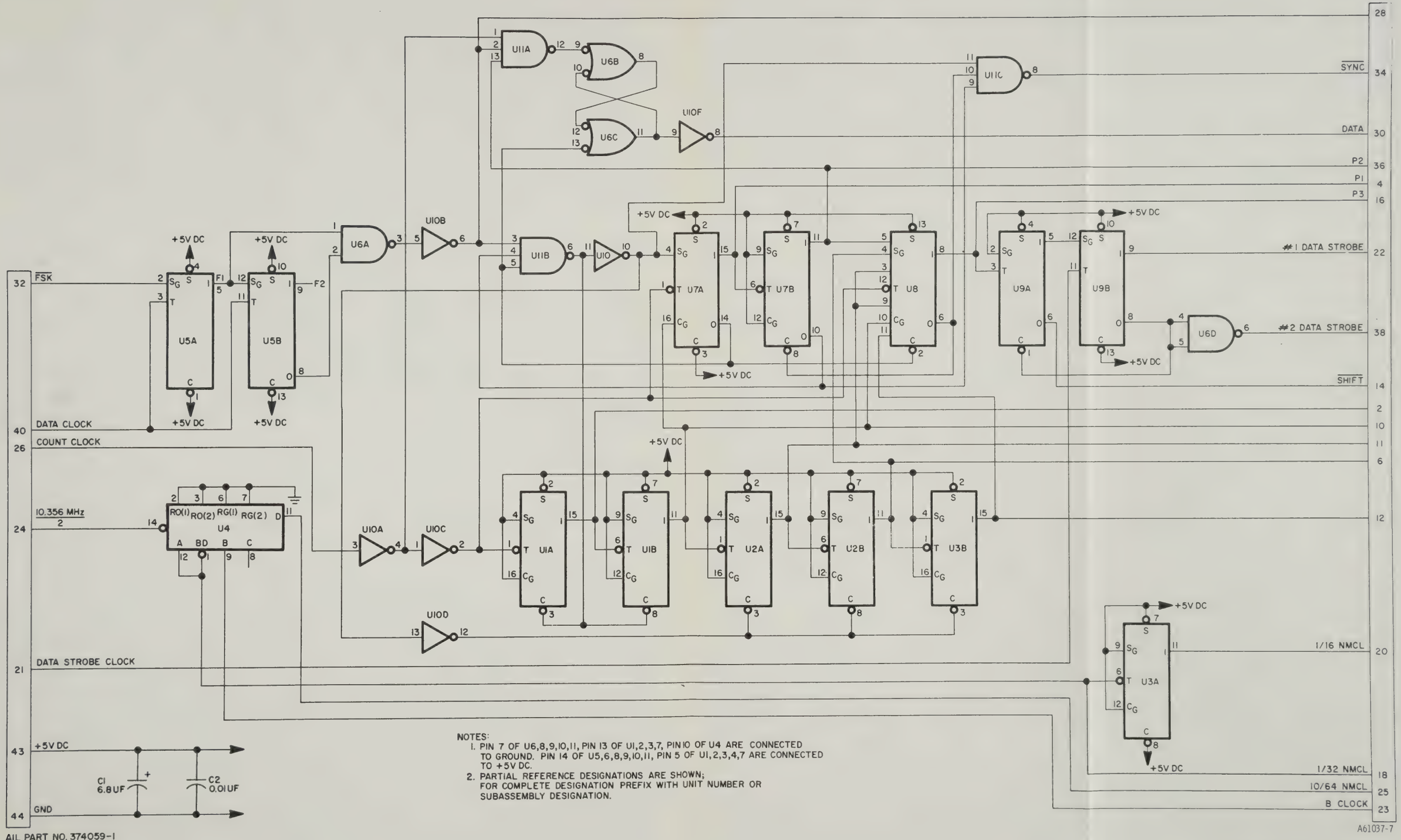


AIL PART NO. 374262-1

NOTES:
1. PIN 7 OF U1 IS CONNECTED TO GROUND. PIN 14 OF U1 THRU U7 IS CONNECTED TO +5V DC
2. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN FOR COMPLETE DESIGNATION PREFIX WITH UNIT NUMBER OR SUB ASSEMBLY DESIGNATION.

A61037-6

FIGURE 6. FCL, CIRCUIT CARD SCHEMATIC

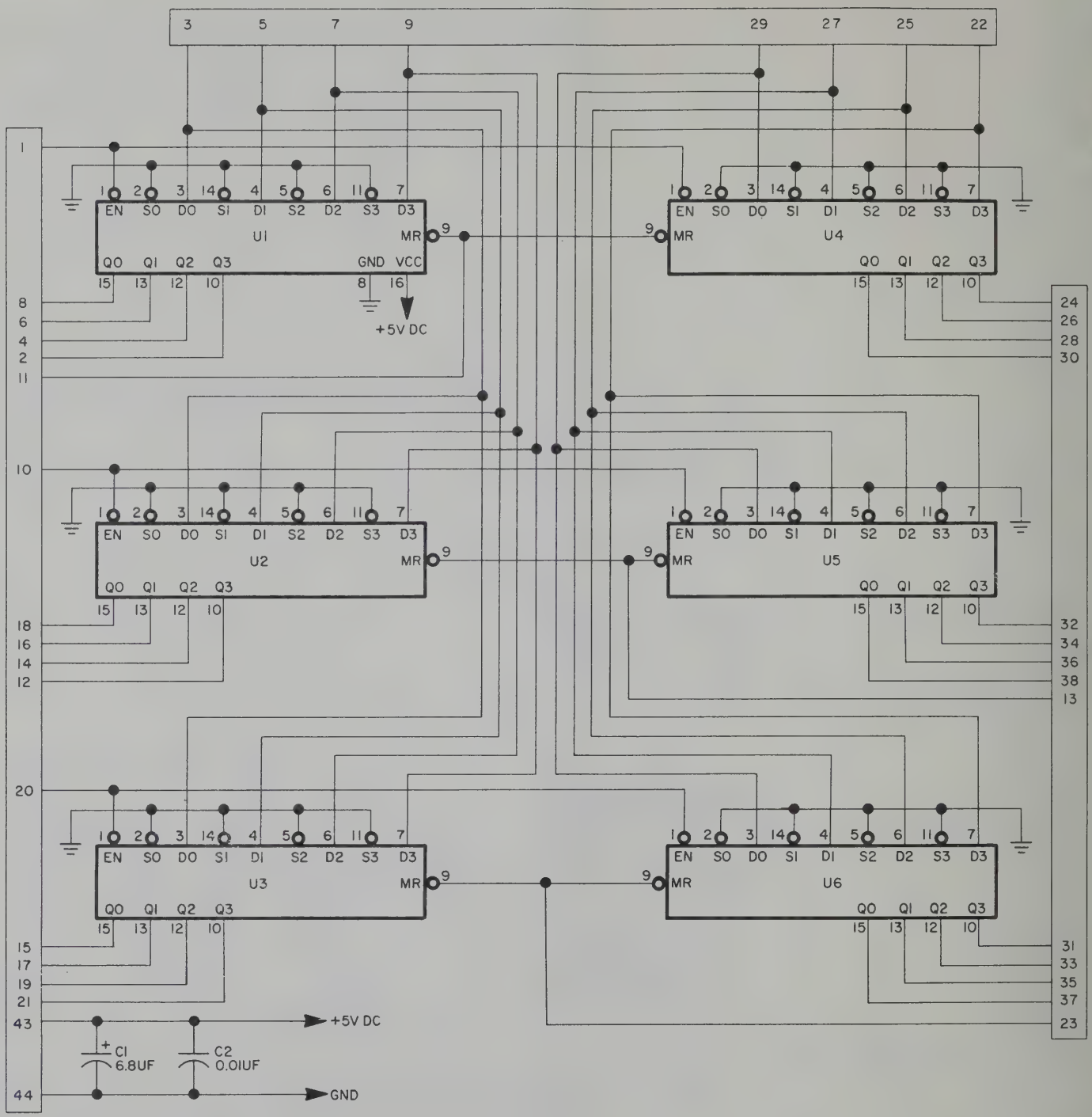


NOTES:
1. PIN 7 OF U6,8,9,10,11, PIN 13 OF U1,2,3,7, PIN 10 OF U4 ARE CONNECTED TO GROUND. PIN 14 OF U5,6,8,9,10,11, PIN 5 OF U1,2,3,4,7 ARE CONNECTED TO +5V DC.
2. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN; FOR COMPLETE DESIGNATION PREFIX WITH UNIT NUMBER OR SUBASSEMBLY DESIGNATION.

A61037-7

AIL PART NO. 374059-1

FIGURE 7. FSK, CIRCUIT CARD SCHEMATIC

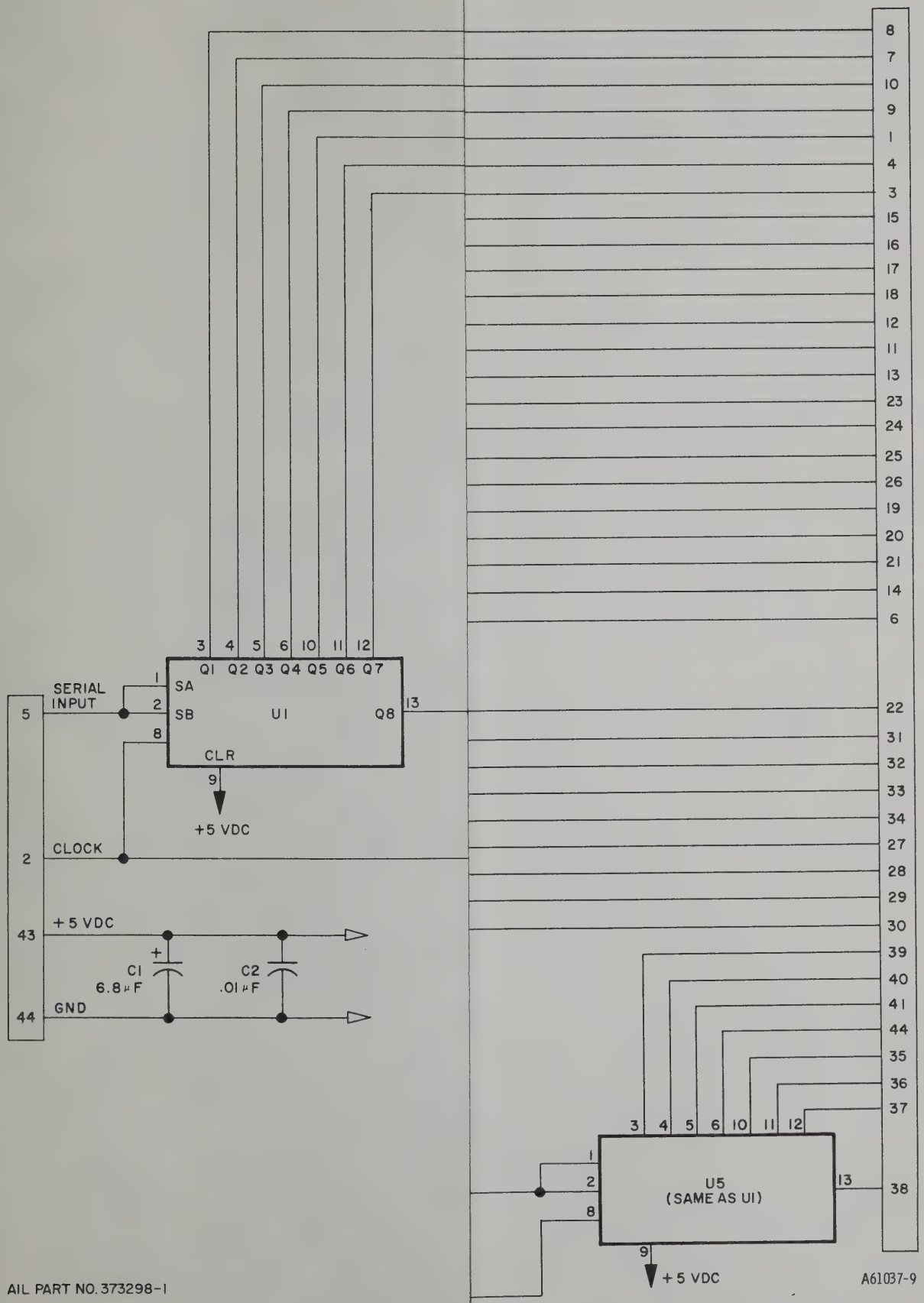


NOTES:
1. PIN 8 OF U1 THROUGH U6 ARE CONNECTED TO GROUND. PIN 16 OF U1 THROUGH U6 ARE CONNECTED TO +5V DC.
2. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN; FOR COMPLETE DESIGNATION PREFIX WITH UNIT NUMBER OR SUBASSEMBLY DESIGNATIONS.

A61037-8

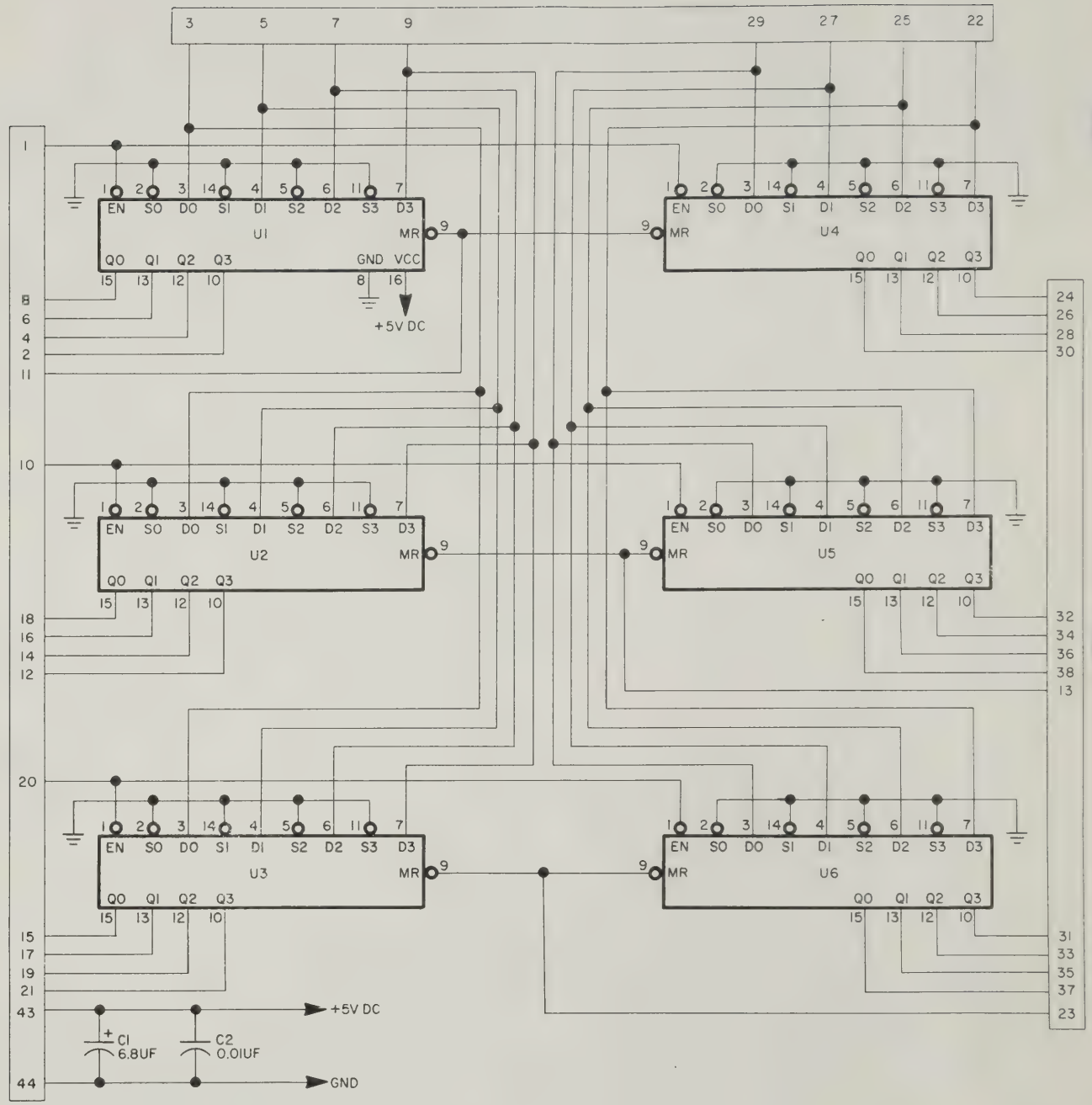
AIL PART NO. 373673-1

FIGURE 8. DDS, CIRCUIT CARD SCHEMATIC



AIL PART NO. 373298-1

FIGURE 9. DDL, CIRCUIT CARD SCHEMATIC

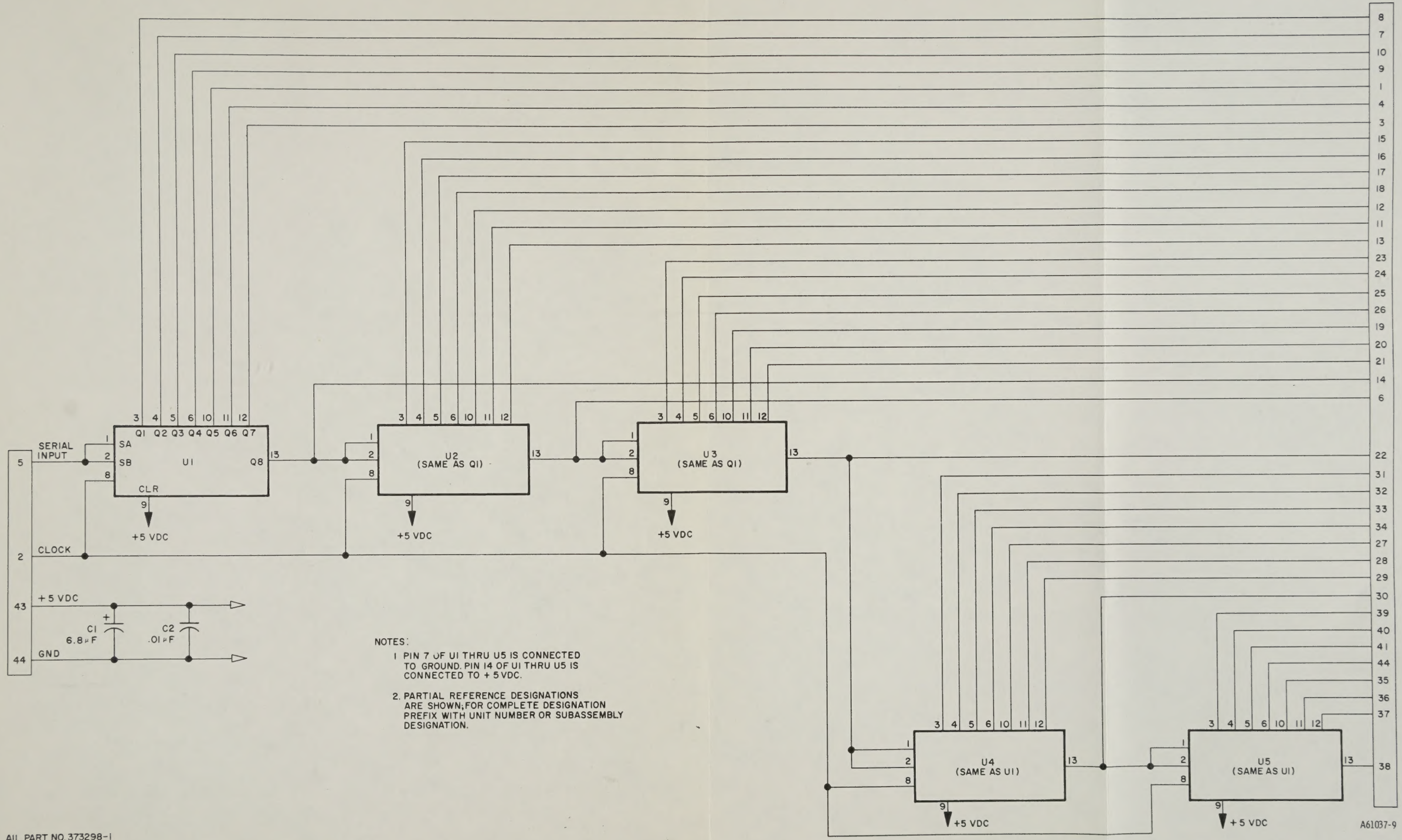


NOTES:
1. PIN 8 OF U1 THROUGH U6 ARE CONNECTED TO GROUND. PIN 16 OF U1 THROUGH U6 ARE CONNECTED TO +5V DC.
2. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN; FOR COMPLETE DESIGNATION PREFIX WITH UNIT NUMBER OR SUBASSEMBLY DESIGNATIONS.

A61037-8

AIL PART NO. 373673-1

FIGURE 8. DDS, CIRCUIT CARD SCHEMATIC

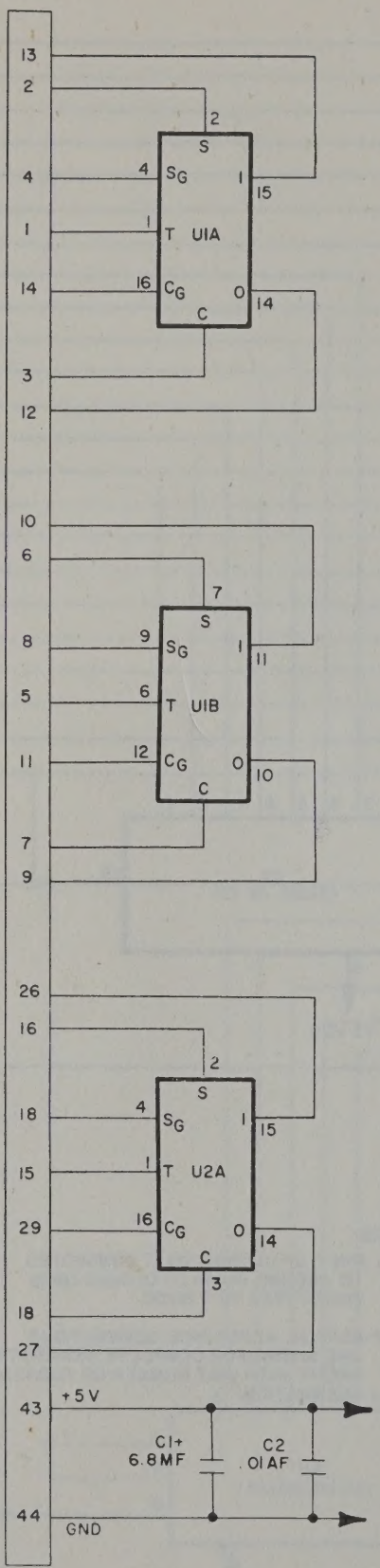


NOTES:

1. PIN 7 OF U1 THRU U5 IS CONNECTED TO GROUND. PIN 14 OF U1 THRU U5 IS CONNECTED TO + 5 VDC.
2. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN; FOR COMPLETE DESIGNATION PREFIX WITH UNIT NUMBER OR SUBASSEMBLY DESIGNATION.

AIL PART NO. 373298-1

FIGURE 9. DDL, CIRCUIT CARD SCHEMATIC



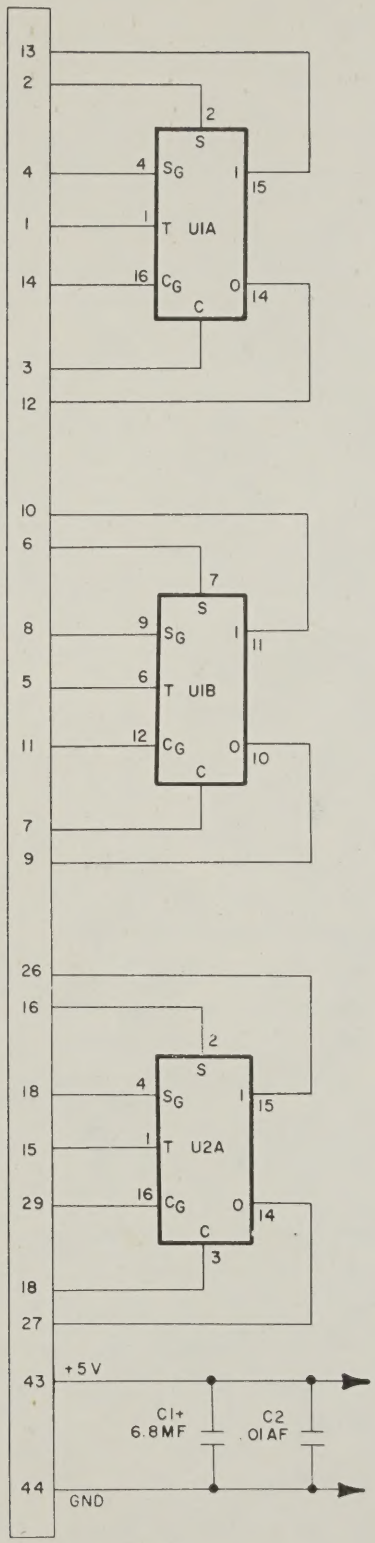
AIL PART NO. 373621-1

NOTES:

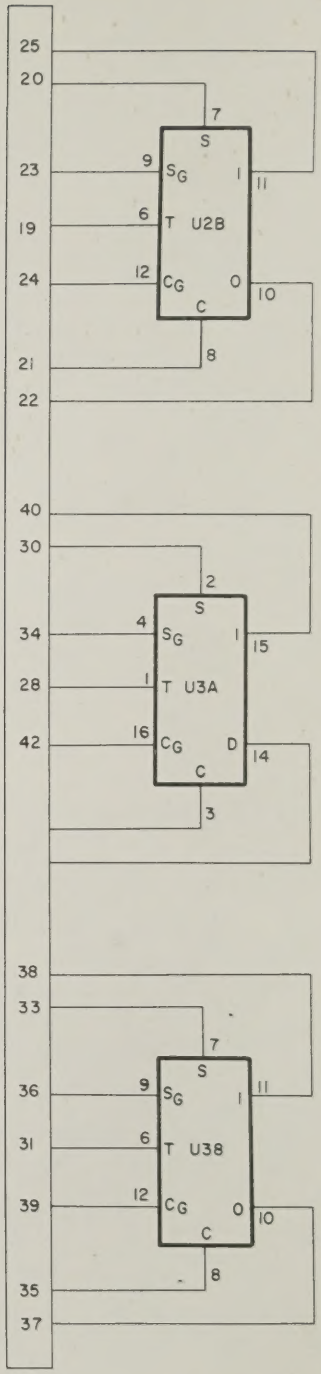
1. PIN 13 OF U1 THRU U3 ARE CONNECTED TO GROUND PIN 5 OF U1 THRU U3 ARE CONNECTED TO +5VDC
2. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN, FOR COMPLETE DESIGNATION PREFIX WITH UNIT NUMBER OR SUBASSEMBLY DESIGNATION

A61037-10

FIGURE 10. CFF, CIRCUIT CARD SCHEMATIC



AIL PART NO. 373621-1



NOTES

1. PIN 13 OF U1 THRU U3 ARE CONNECTED TO GROUND PIN 5 OF U1 THRU U3 ARE CONNECTED TO +5VDC
2. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN, FOR COMPLETE DESIGNATION PREFIX WITH UNIT NUMBER OR SUBASSEMBLY DESIGNATION

A61037-10

FIGURE 10. CFF, CIRCUIT CARD SCHEMATIC